

MODEL NAME :FDX40  
PCB NO :LA-J261P  
BOM P/N :431AJS31LXX

Comet Lake U42 V1  
2020-03-27  
REV : 1.0 (A00)

@ : Nopop Component  
EMI@ : EMI Component  
@EMI@ : EMI Nopop Component  
ESD@ : ESDComponent  
@ESD@ : ESD Nopop Component  
RF@ : RF Component  
@RF@ : RF Nopop Component  
DS3@ : Deep sleep support  
NDS3@ : NDS3 support  
@NDS3@ : NDS3 Nopop Component  
CXDP@ : XDP Component  
RTD3@ : RTD3 Component  
@RTD3@ : RTD3 Nopop Component  
NRTD3@ : RTD3 Component  
VPRO@ : vPro Component  
NVPRO@ : Non-vPro Component  
JUMP@ : Jump solder and short  
@JUMP@ : Jump no solder  
5107ES@ : 5107 ES Component  
5107NES@ : 5107 non-ES Component  
CONN@ : Connector Component

AC@ : Intel 9560 WLAN Solder Down Component  
AX@ : Intel AX201 WLAN Solder Down Component  
AXN@ : Intel AX201(N) WLAN Solder Down  
SDP@ : Single-Die Package DRAM Component  
DDP@ : Dual-Die Package DRAM Component  
S4G@ : Samsung 4GB DRAM Component  
S8G@ : Samsung 8GB DRAM Component  
S16G@ : Samsung 16GB DRAM Component  
S32G@ : Samsung 32GB DRAM Component  
H4G@ : Hynix 4GB DRAM Component  
H8G@ : Hynix 8GB DRAM Component  
H16G@ : Hynix 16GB DRAM Component  
H32G@ : Hynix 32GB DRAM Component  
M4G@ : Micron 4GB DRAM Component  
M4GN@ : Micron New 4GB DRAM Component  
M8G@ : Micron 8GB DRAM Component  
M8GN@ : Micron New 8GB DRAM Component  
M16G@ : Micron 16GB DRAM Component  
M16GN@ : Micron New 16GB DRAM Component  
M32G@ : Micron 32GB DRAM Component

Layout Dell logo




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REV:A00  
PWB:CP2JJ

MB PCB	
Part Number	Description
DAB0005M010	PCB 2UW LA-J261P REV1 MB

Power CKT :RIVERSIDE\_PVT\_POWER\_200305  
GPIO map : X11\_CML\_U\_CSLP GPIO map Rev0.7\_20190919

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Title

Cover Sheet

Size

Document Number

LA-J261p

Rev

1.0

Date

Friday, March 27, 2020

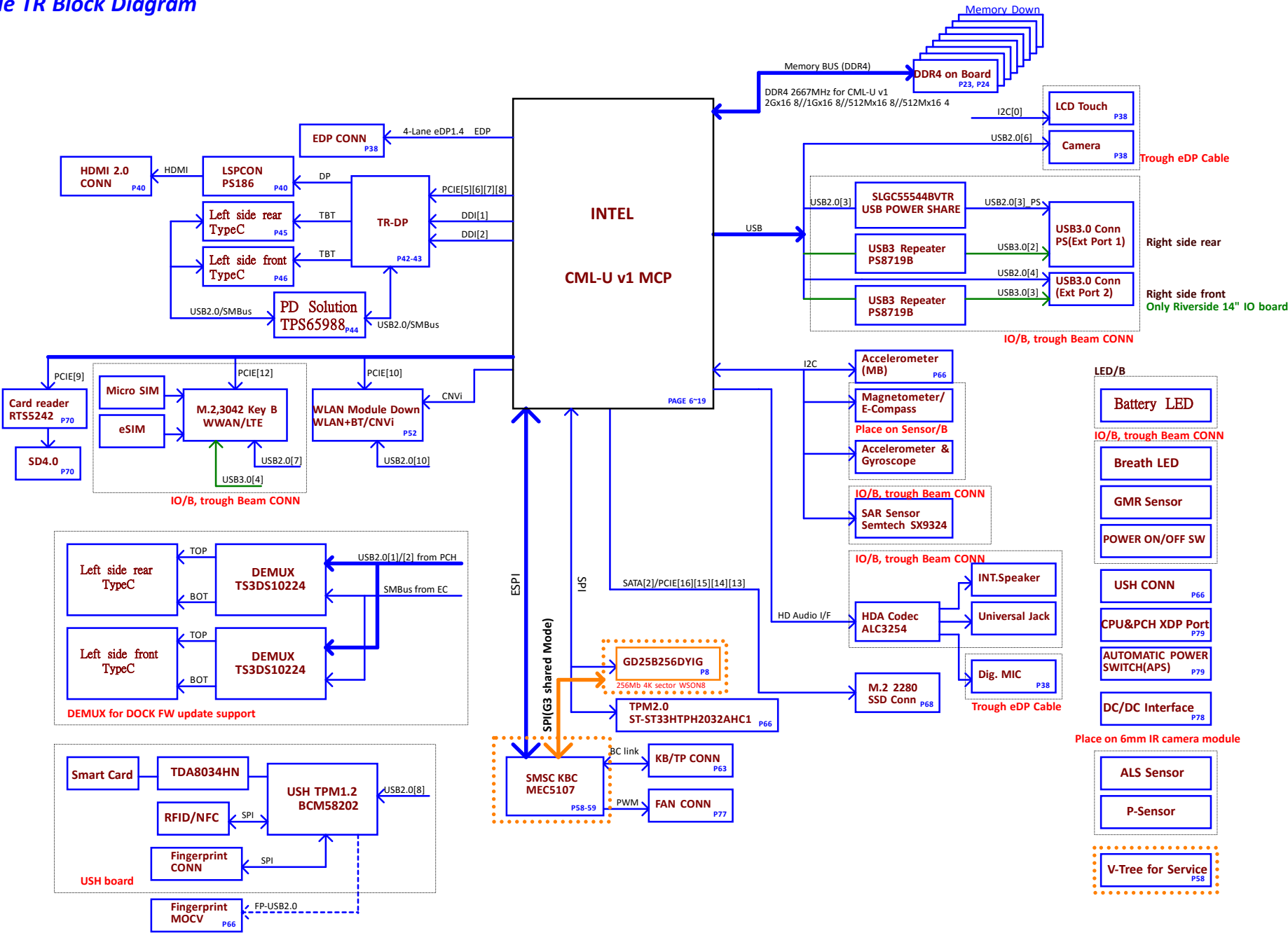
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Riverside TR Block Diagram



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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S0ix/Moff	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S0ix (Suspend to RAM) / M-OFF	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

USB3.0	Gbe	PCIE	SATA	DESTINATION
USB3.0-1		PCIE-1		N/A
USB3.0-2		PCIE-2		JUSB1-->Right Rear
USB3.0-3		PCIE-3		JUSB2-->Right Front
USB3.0-4		PCIE-4		M.2 3042(LTE)
USB3.0-5		PCIE-5		Titan Ridge - DP
USB3.0-6		PCIE-6		
		PCIE-7		
		PCIE-8		
		PCIE-9		
		PCIE-10		Card Reader
		PCIE-11	SATA-0	Solder Down 1216(WLAN)
		PCIE-12	SATA-1	N/A
		PCIE-13		M.2 3042(LTE)
		PCIE-14		M.2 2280 SSD
		PCIE-15		
		PCIE-16	SATA-2	

USB PORT#	DESTINATION
1	Type-C Port1
2	Type-C Port2
3	JUSB1-->Right Rear
4	JUSB2-->Right Front
5	NA
6	Camera
7	M.2 3042(WWAN)
8	USH
9	Reserved for FPR in PB
10	Solder Down 1216(BT)

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.05V_PRIM	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.05V_VCCSTG	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +1.2V_RUN
S0	ON	ON	ON
S0ix	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	ON	OFF	OFF

Figure 105. High Speed I/O (HSIO) Lane Multiplexing in PCH-LP (U)

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIE * #7	PCIE * #8	PCIE * #9	PCIE * #10	PCIE * #11	PCIE * #12	PCIE * #13	PCIE * #14	PCIE * #15	PCIE * #16
	PCIE * #1	PCIE * #2	PCIE * #3	PCIE * #4	PCIE * #5	PCIE * #6	Gbe	Gbe	Gbe	SATA 0	SATA 1a	Gbe	Gbe	SATA 1b	SATA 2	SATA 2
Intel® RST Support	No Support				No Support				Yes				Yes			

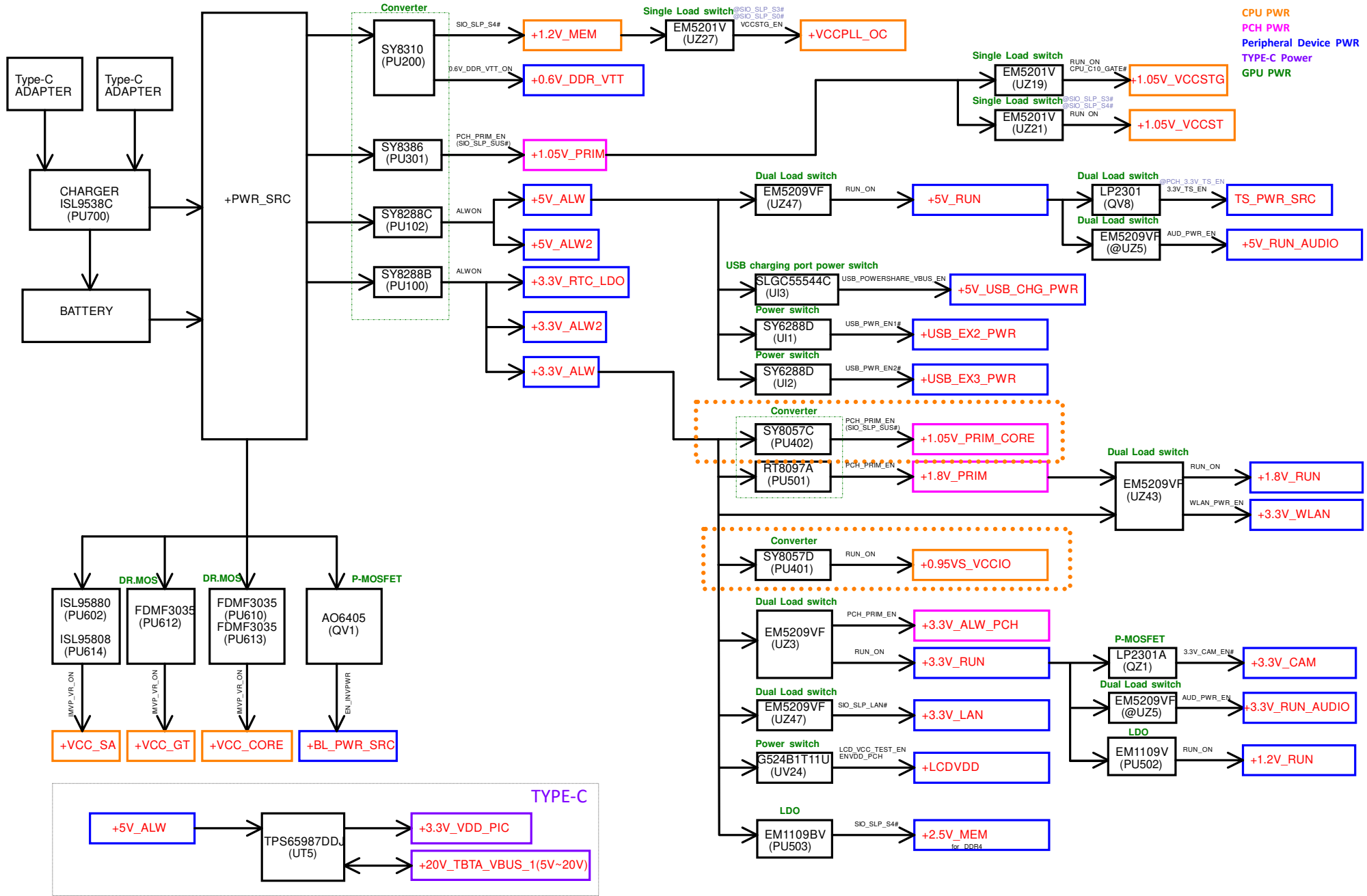
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Title		Port assignment	
Size	Document Number	LA-J261p	
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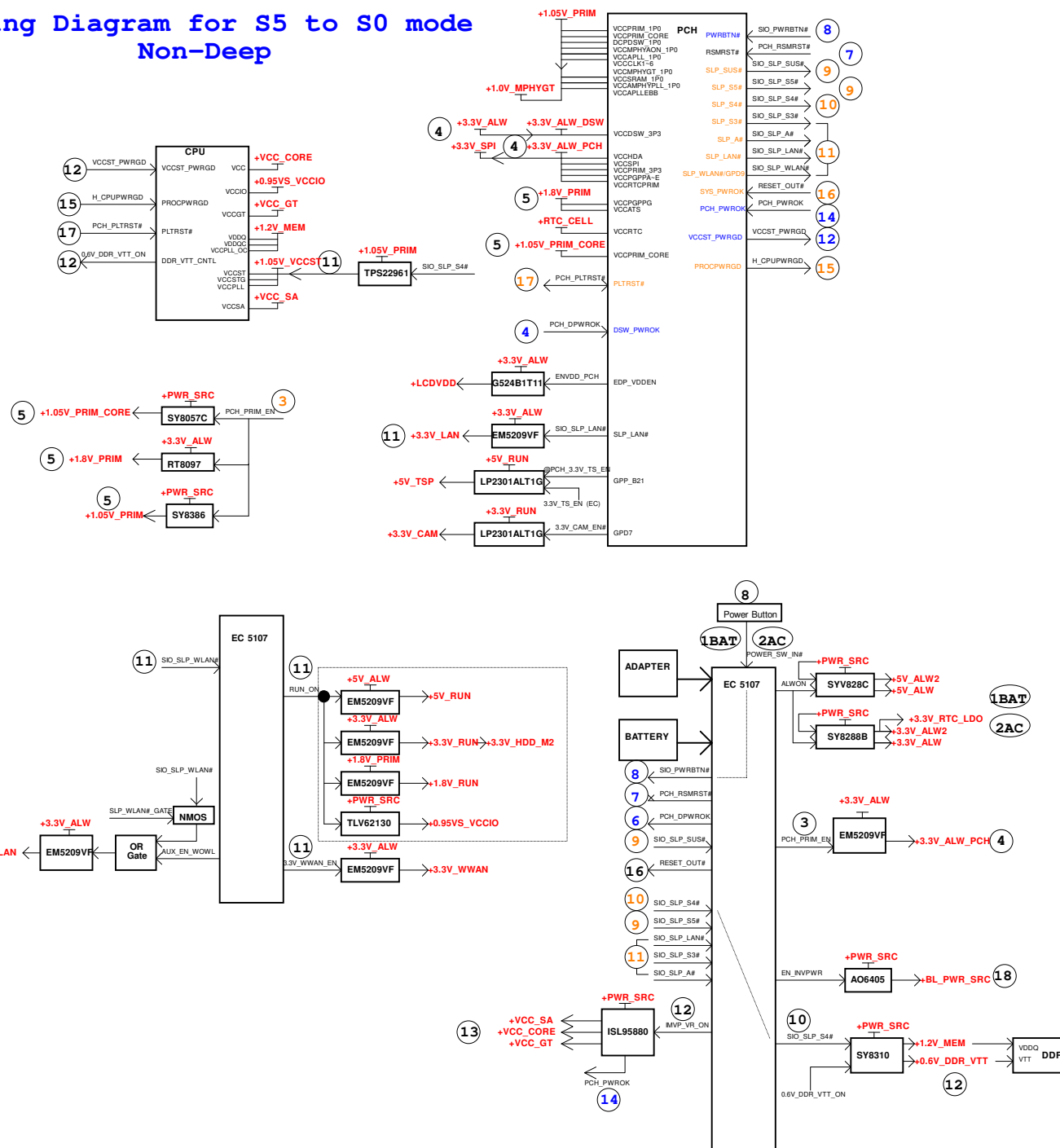
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**Power rails**

**LA-J261p**

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Size	Document	Number	1.0	
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### Timing Diagram for S5 to S0 mode Non-Deep



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### Power Sequence

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	LA-1261p

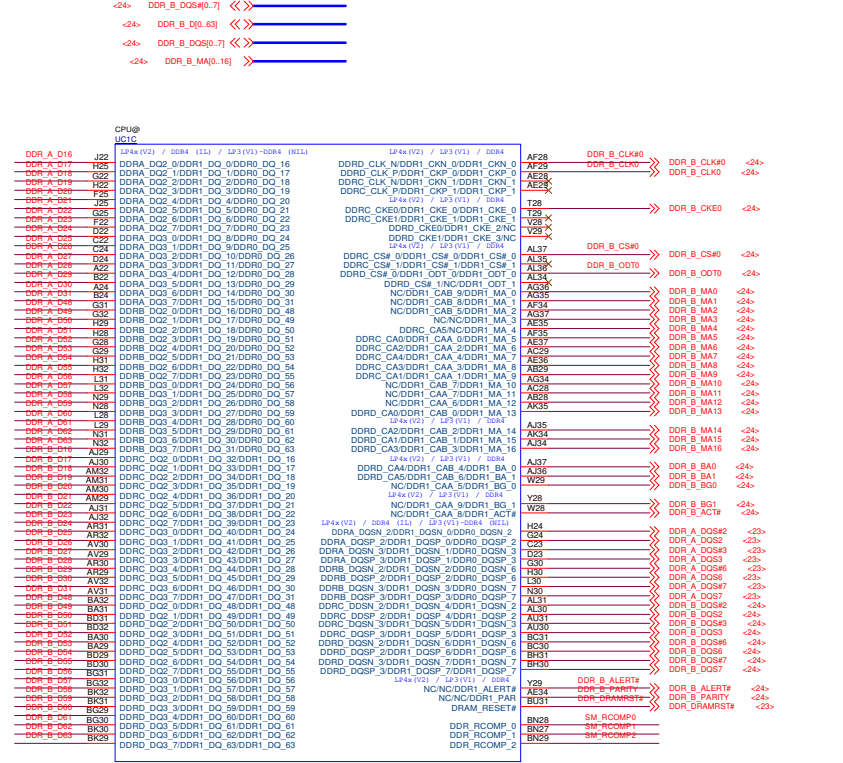
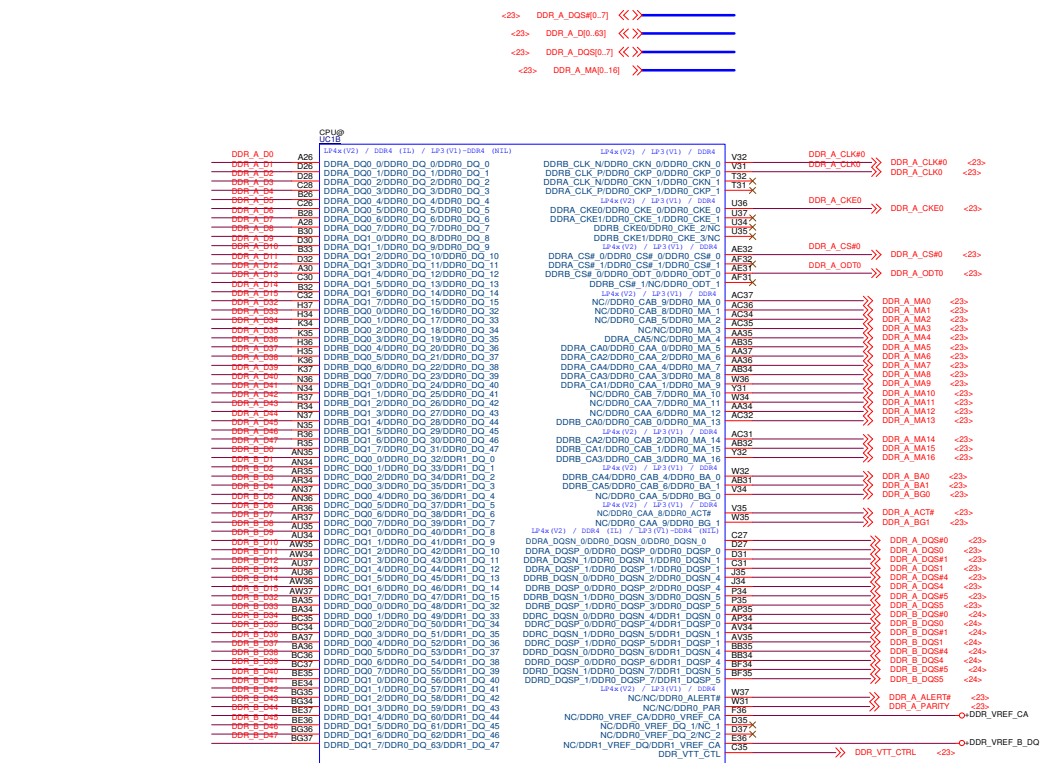
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DDR4, Ballout for side by side(Non-Interleave)



DDR4 COMPENSATION SIGNALS

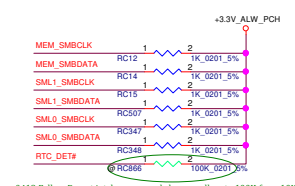
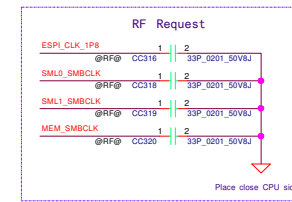
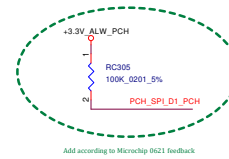
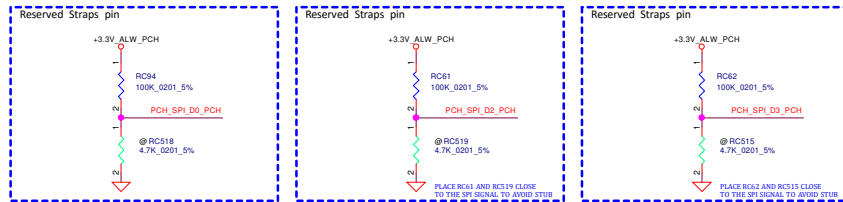


CAD Note:  
Trace width=12~15 mil, Spacing=20 mils  
Max trace length= 500 mil

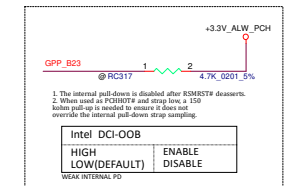
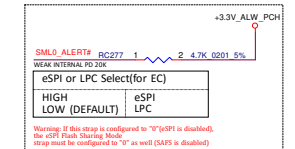
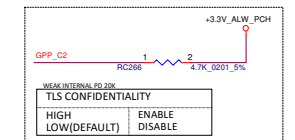
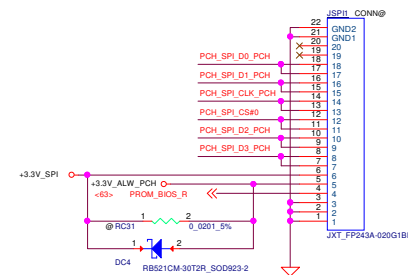
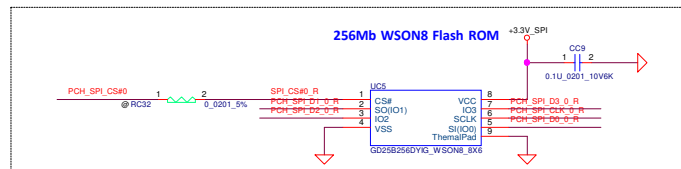
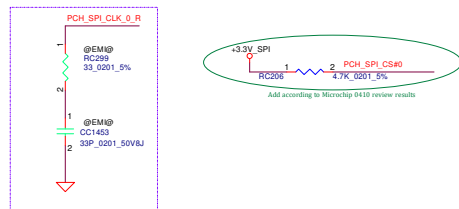
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CPU(2/14)DDR4	
LA-J261P	
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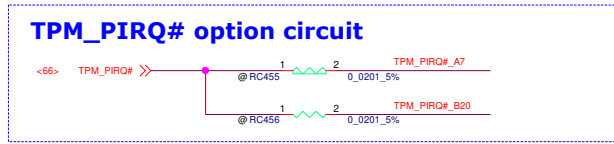
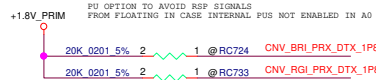
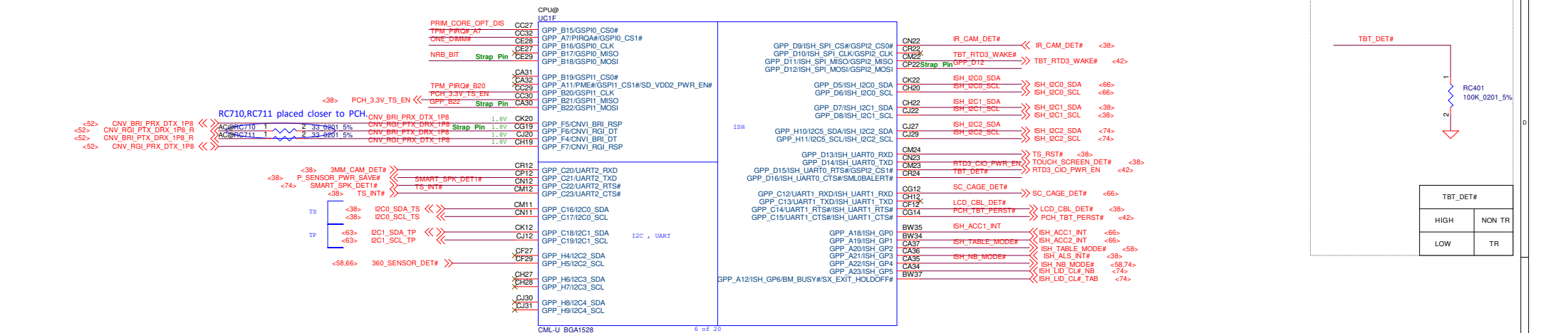
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[illegible]

BIOS ROM (32MB)	GIGADEVICE; GD25B256YIG WSON8; WINBOND; W25Q256JVEIQ WSON8;	ODM
BIOS ROM (16MB)	Dell Approved PN's	ODM

[illegible]

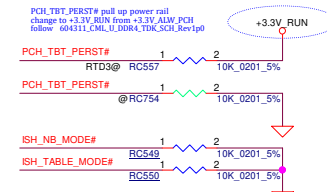
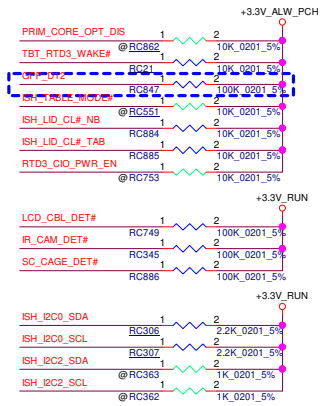
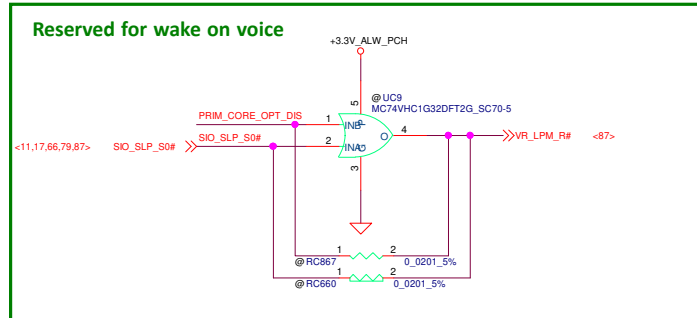
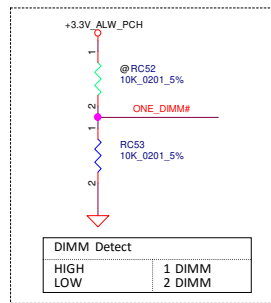
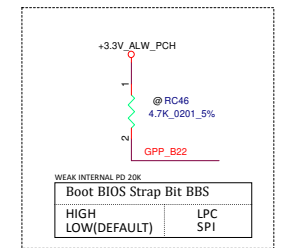
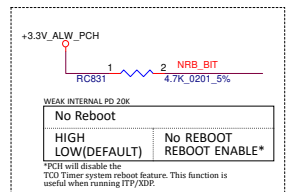
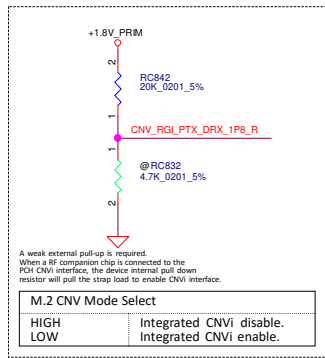




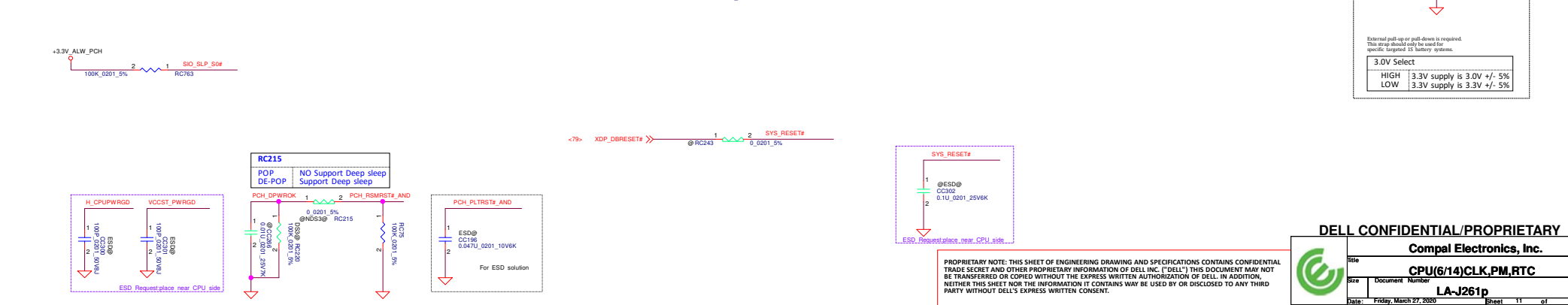
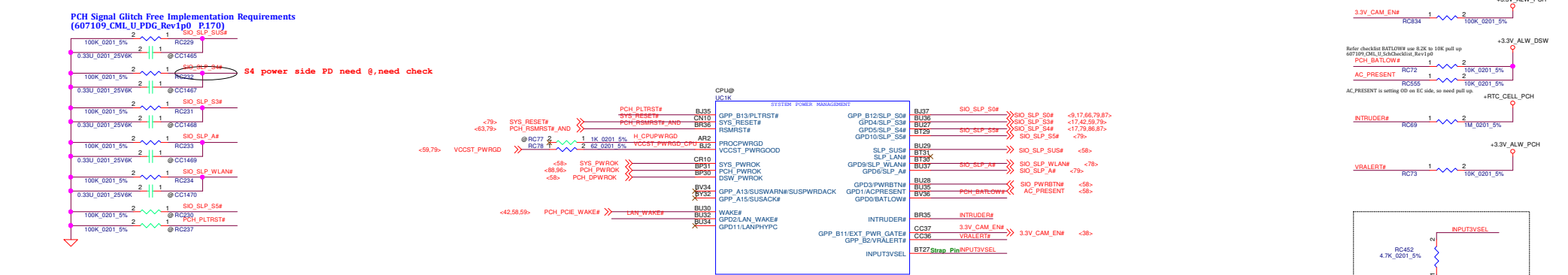
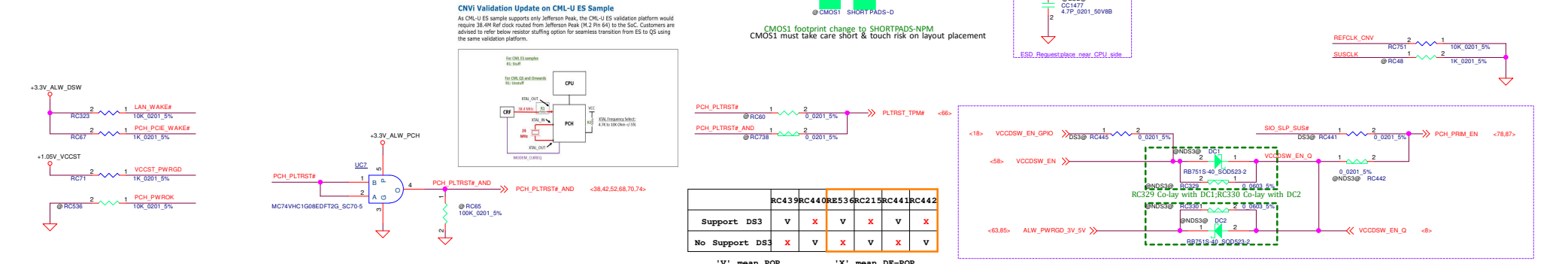
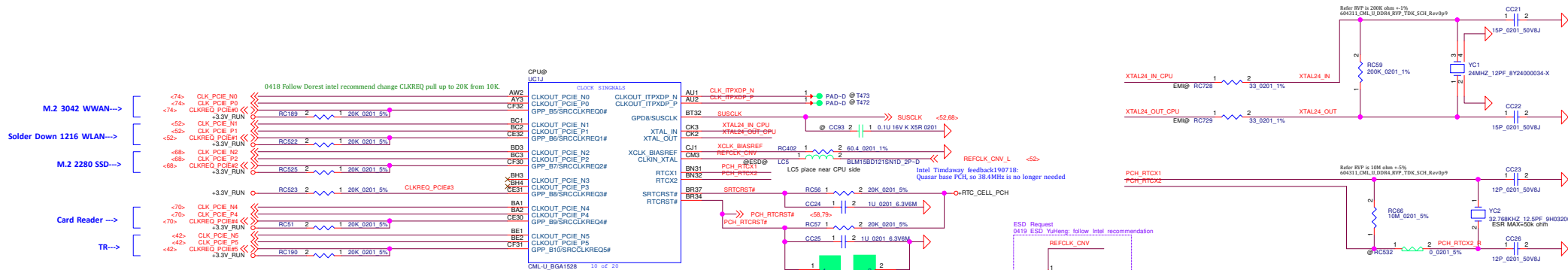
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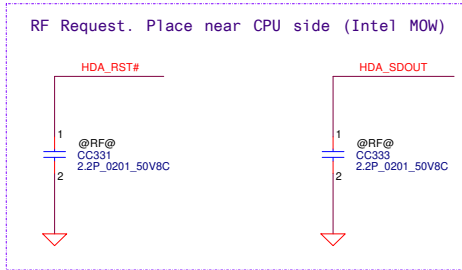
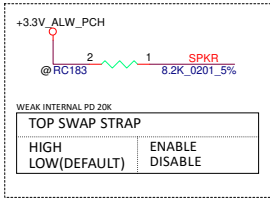
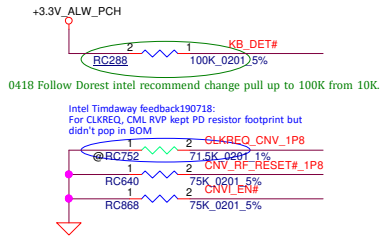
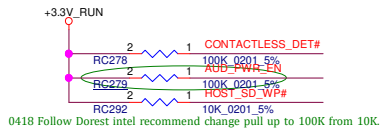
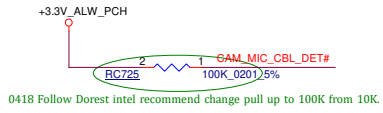
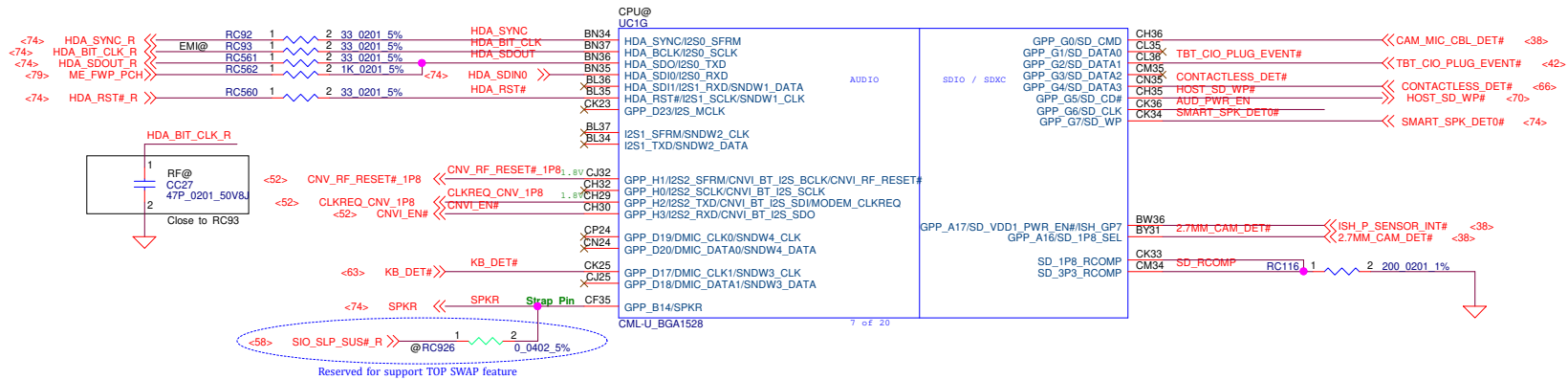
External pull-up is required. Recommend 100 kohm if pulled up to 3.3V or 75 kohm if pulled up to 1.8V.

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.









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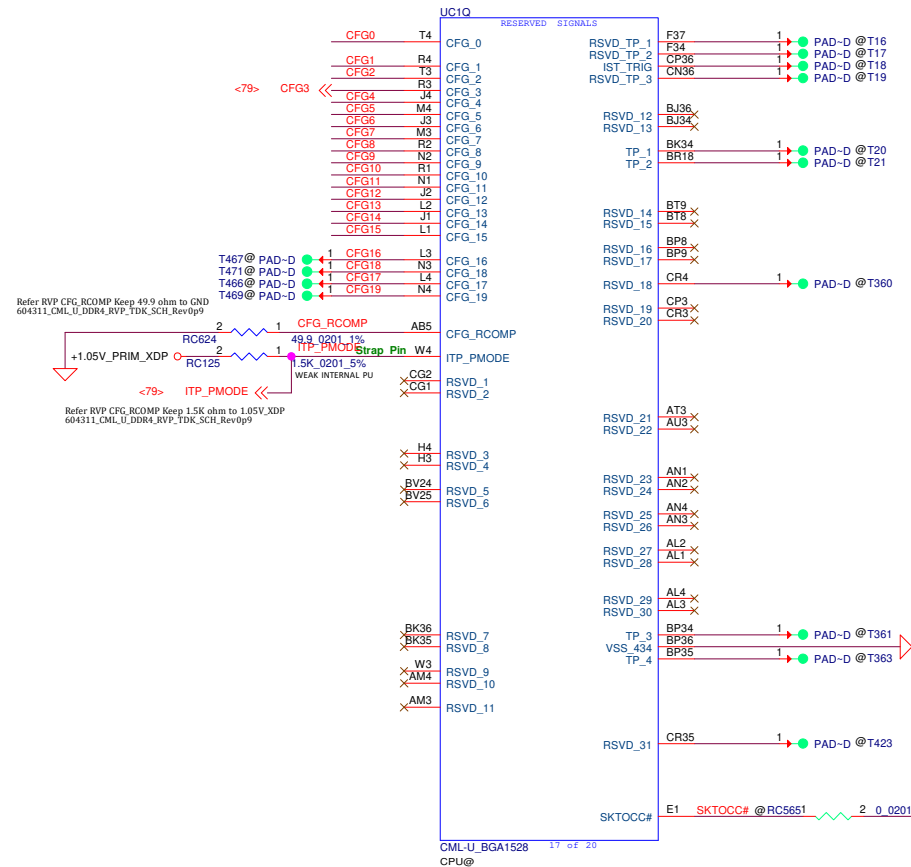
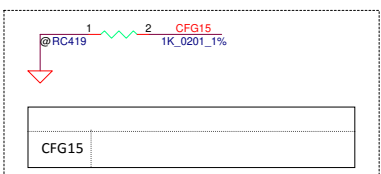
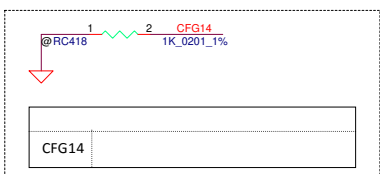
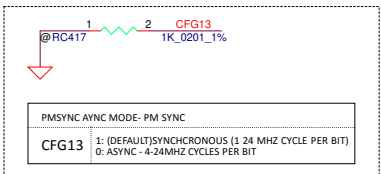
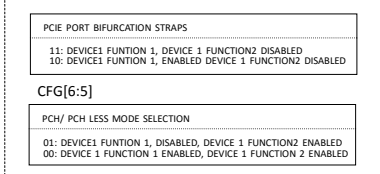
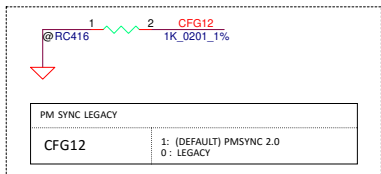
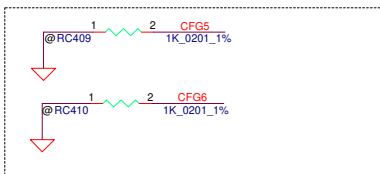
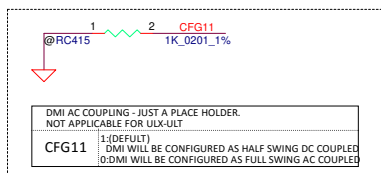
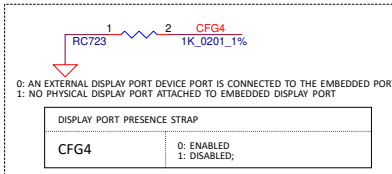
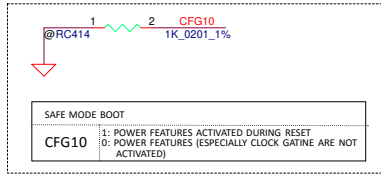
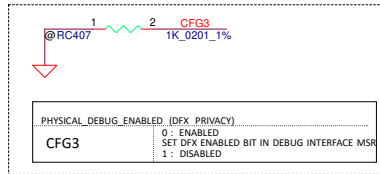
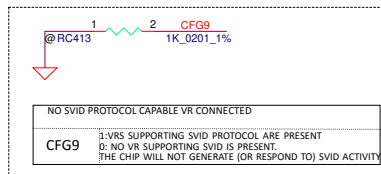
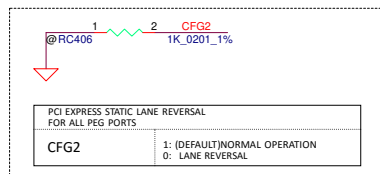
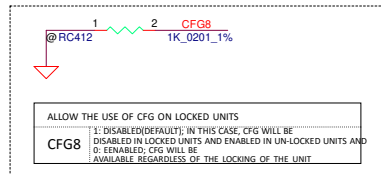
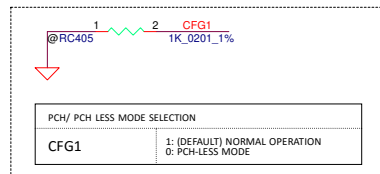
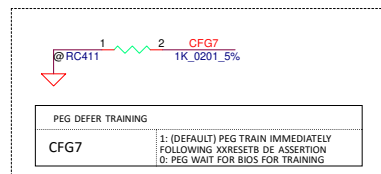
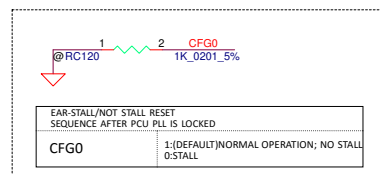
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Title: **CPU(7/14)MISC,JTAG,HDA,SDIO**

Size: **LA-J261p** Rev: **1.0**

Date: **Friday, March 27, 2020** Sheet: **12** of **106**



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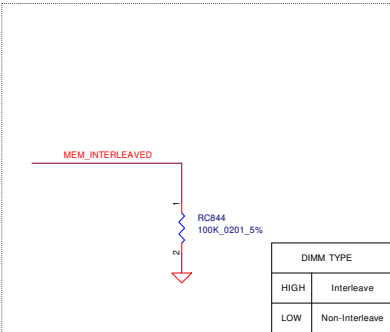
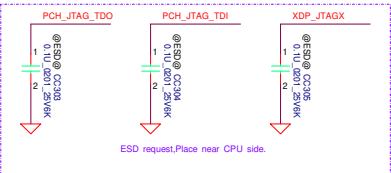
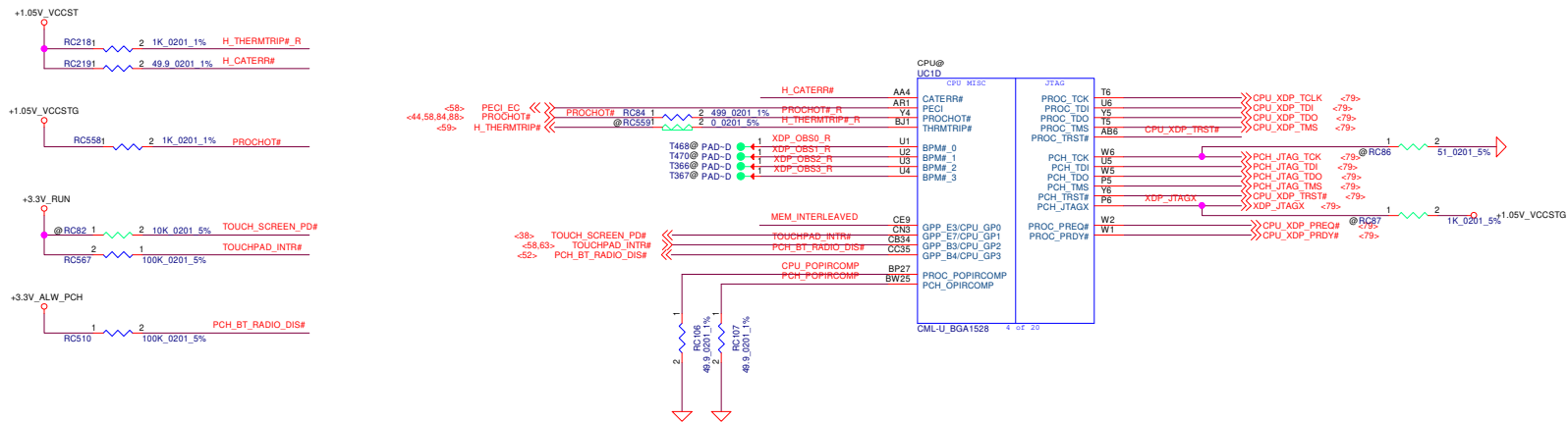
CPU(8/14)CFG,RSVD

**LA-J261p**

1.0

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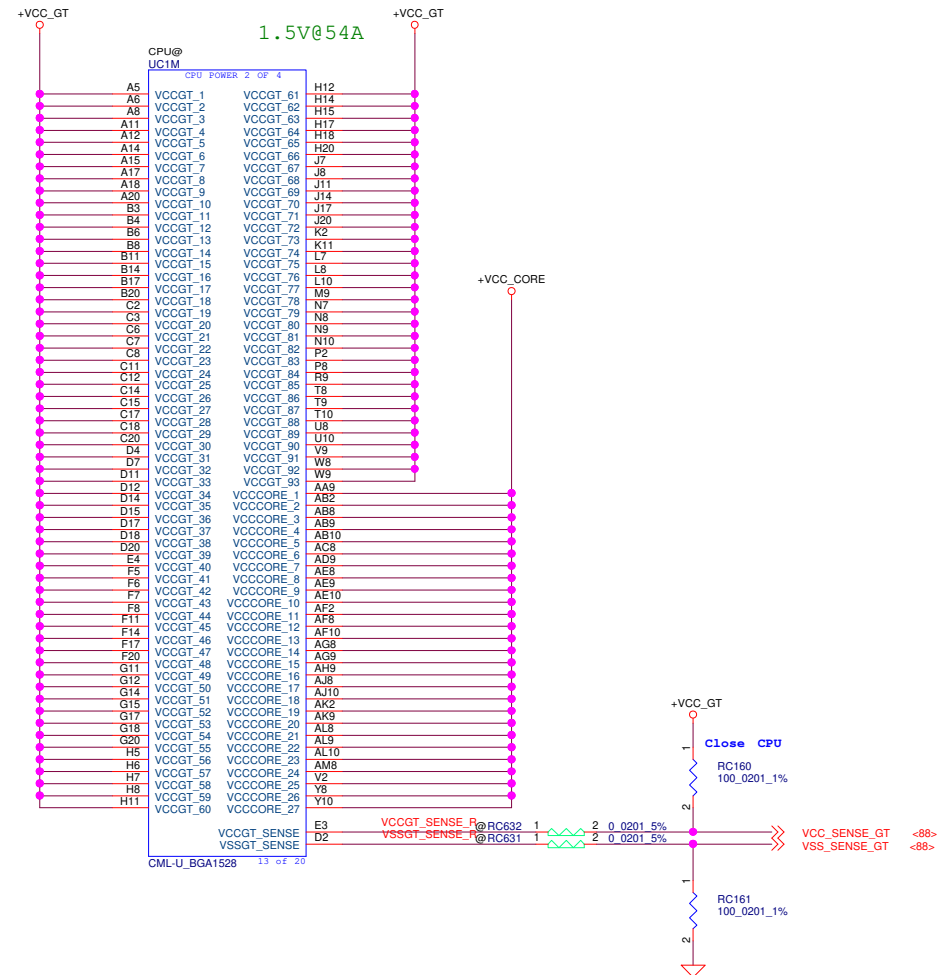


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+VCCGT: 0.55~1.5V, 54A  
+VCCGTx : 0.55~1.5V, 7A



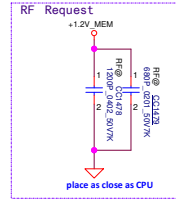
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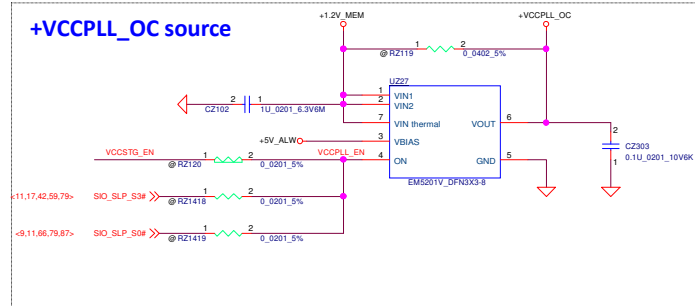
Title			Rev
CPU(11/14)PWR-VCCGT			1.0
Size	Document Number	LA-J261p	
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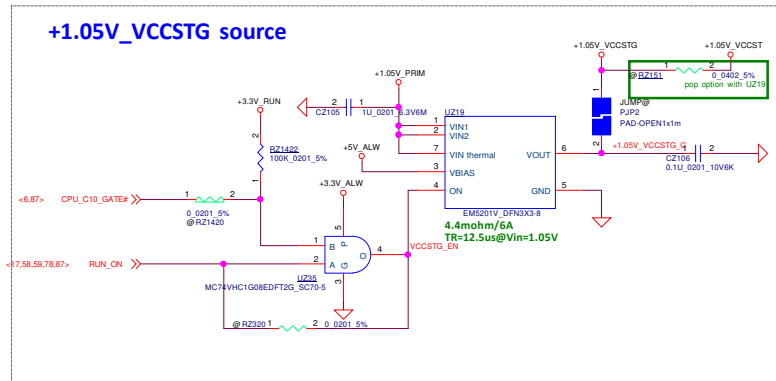
**+1.2V\_DDR: 1.2V, 3.5A**  
**+1.05V\_VCCST: 1.5V, 120mA**  
**+1.05V\_VCCSTG: 1.5V, 40mA**  
**+VCCPLL\_OC: 1.2V, 260mA**  
**+0.95VS\_VCCIO: 0.85~0.95V, 3.1A**  
**+VCC\_SA: 1.15V, 5.1A**



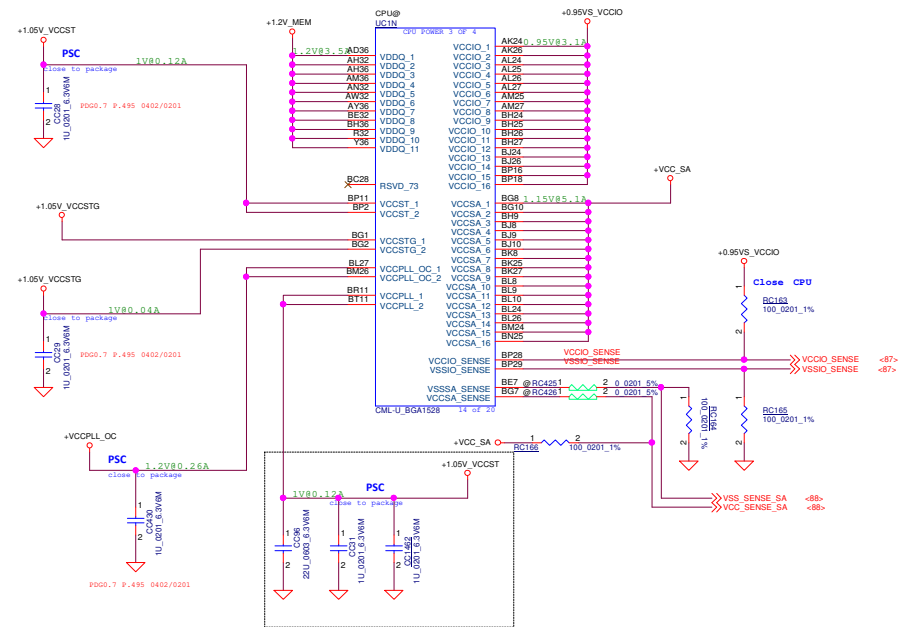
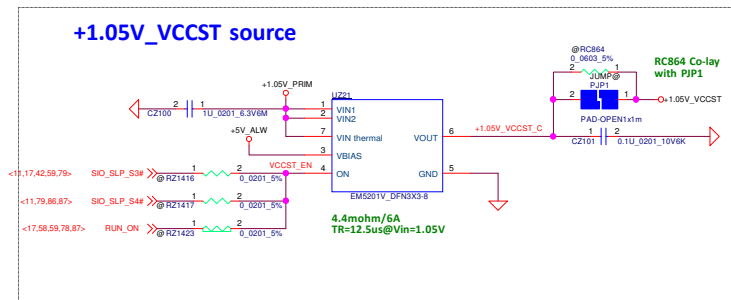
### +VCCPLL\_OC source



### +1.05V\_VCCSTG source



### +1.05V\_VCCST source

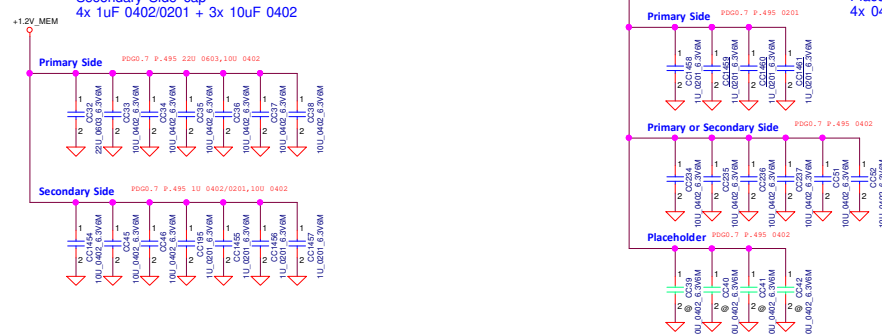


CML U PDG rev1.0 P.537  
 VDDQ:  
 Primary Side cap  
 1x 22uF 0603 + 6x 10uF 0402  
 Secondary Side cap  
 4x 1uF 0402/0201 + 3x 10uF 0402

CML U PDG rev1.0 P.537  
 VCCIO:  
 Primary Side cap  
 4x 1uF 0201

Primary or Secondary Side  
 6x 10uF 0402

Placeholder Only  
 4x 0402



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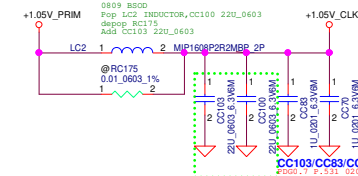
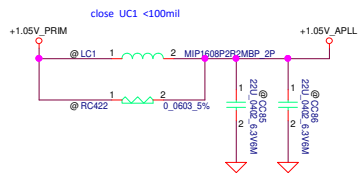
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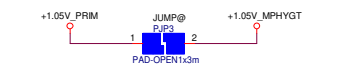
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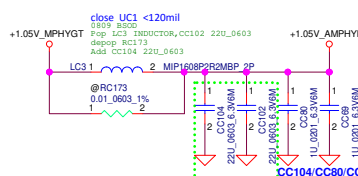
LC1, LC2, LC3 CIS no symbol(SHI0000X800)



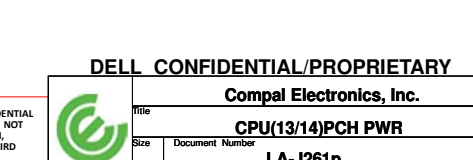
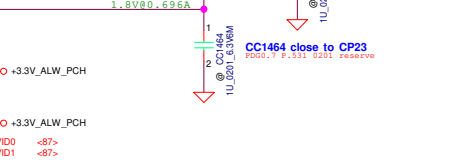
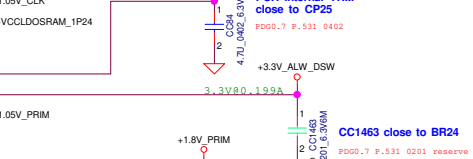
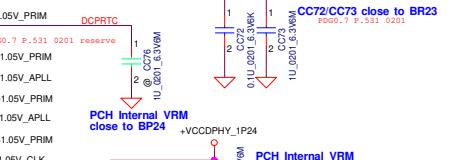
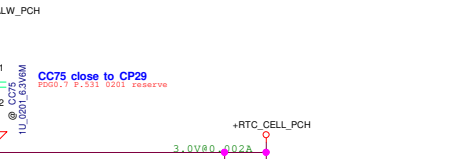
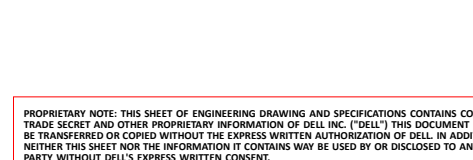
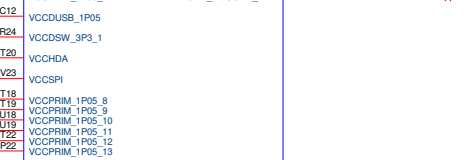
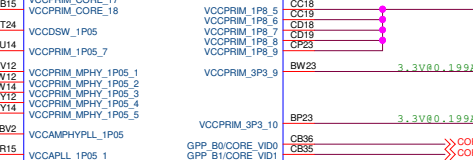
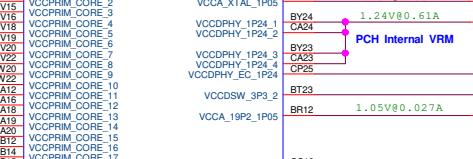
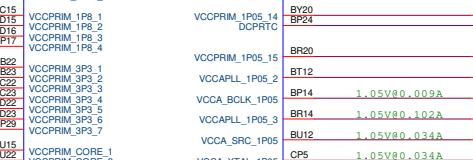
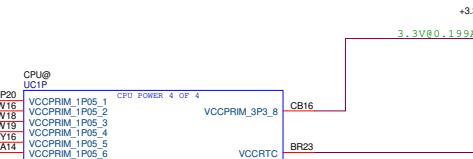
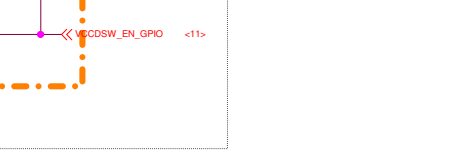
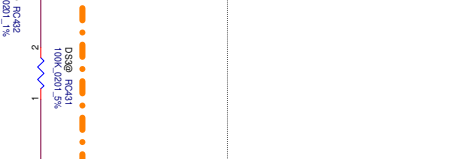
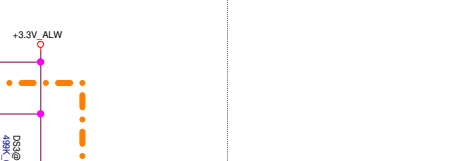
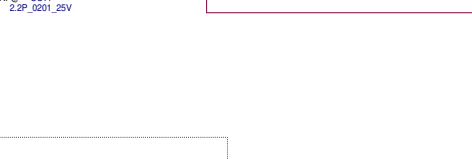
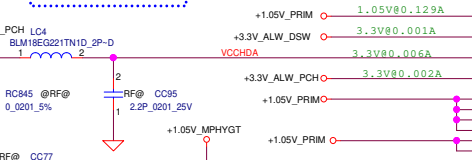
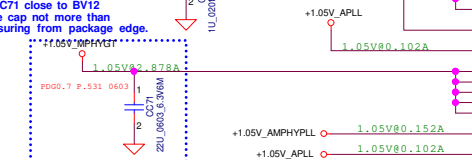
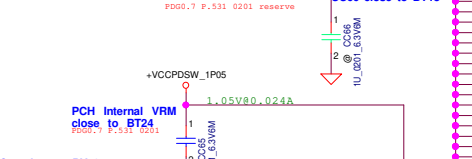
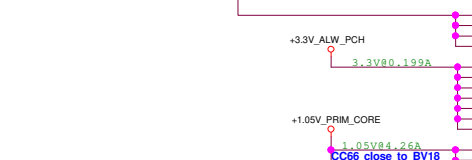
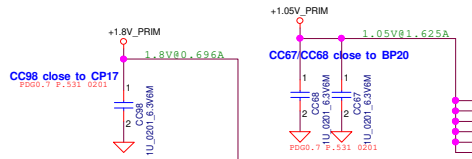
CC100/CC103 one is close to the CPU and the other is far from the CPU.



+1.05V\_MPHYGT source



CC102/CC104 one is close to the CPU and the other is far from the CPU.



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CPU(13/14)PCH PWR

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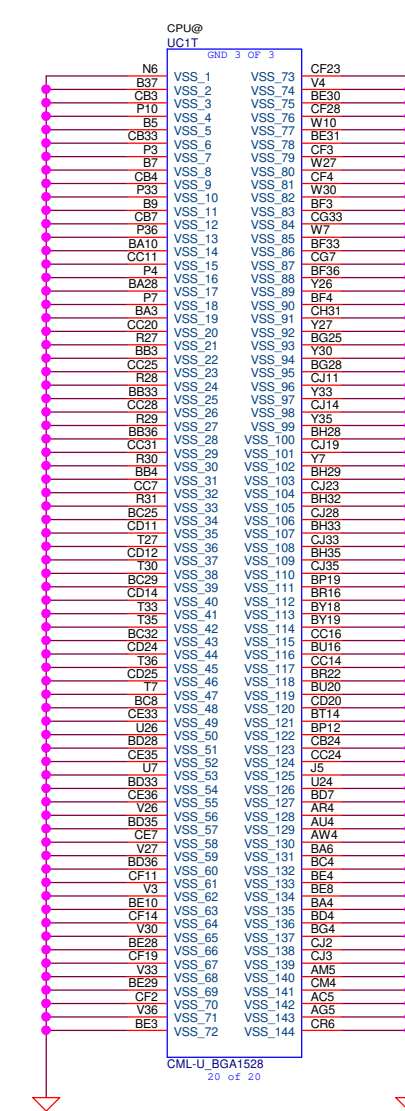
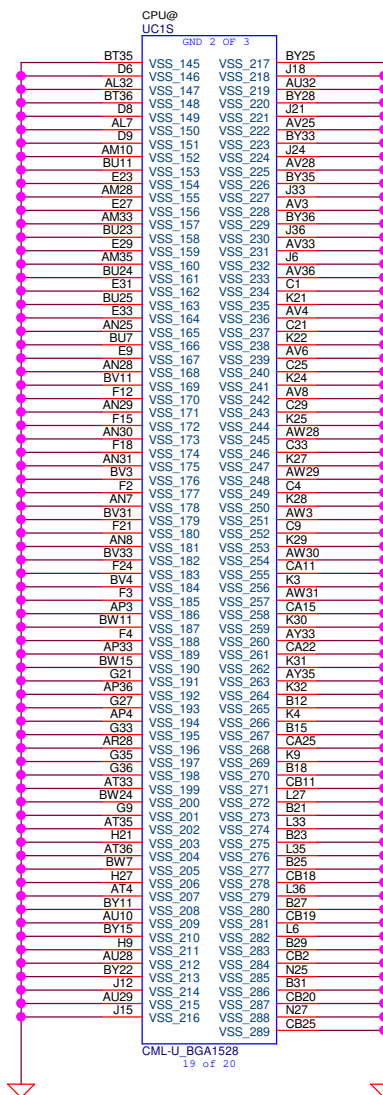
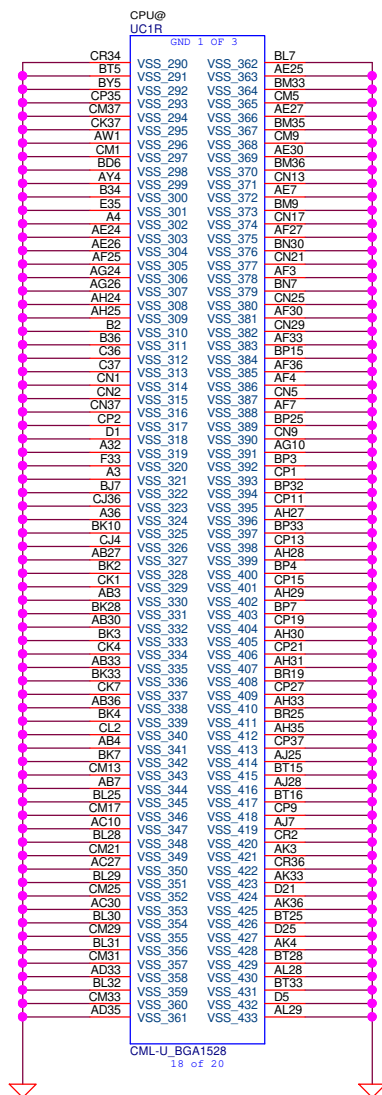
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If support NDS3,depop the part QC6 QC7 RC432 RC433 RC439 RC431


	RC439	RC440	RC441	RC442
Support DS3	V	X	V	X
No Support DS3	X	V	X	V

'V' mean POP,

'X' mean DE-POP



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**MCP(14/14)VSS**  
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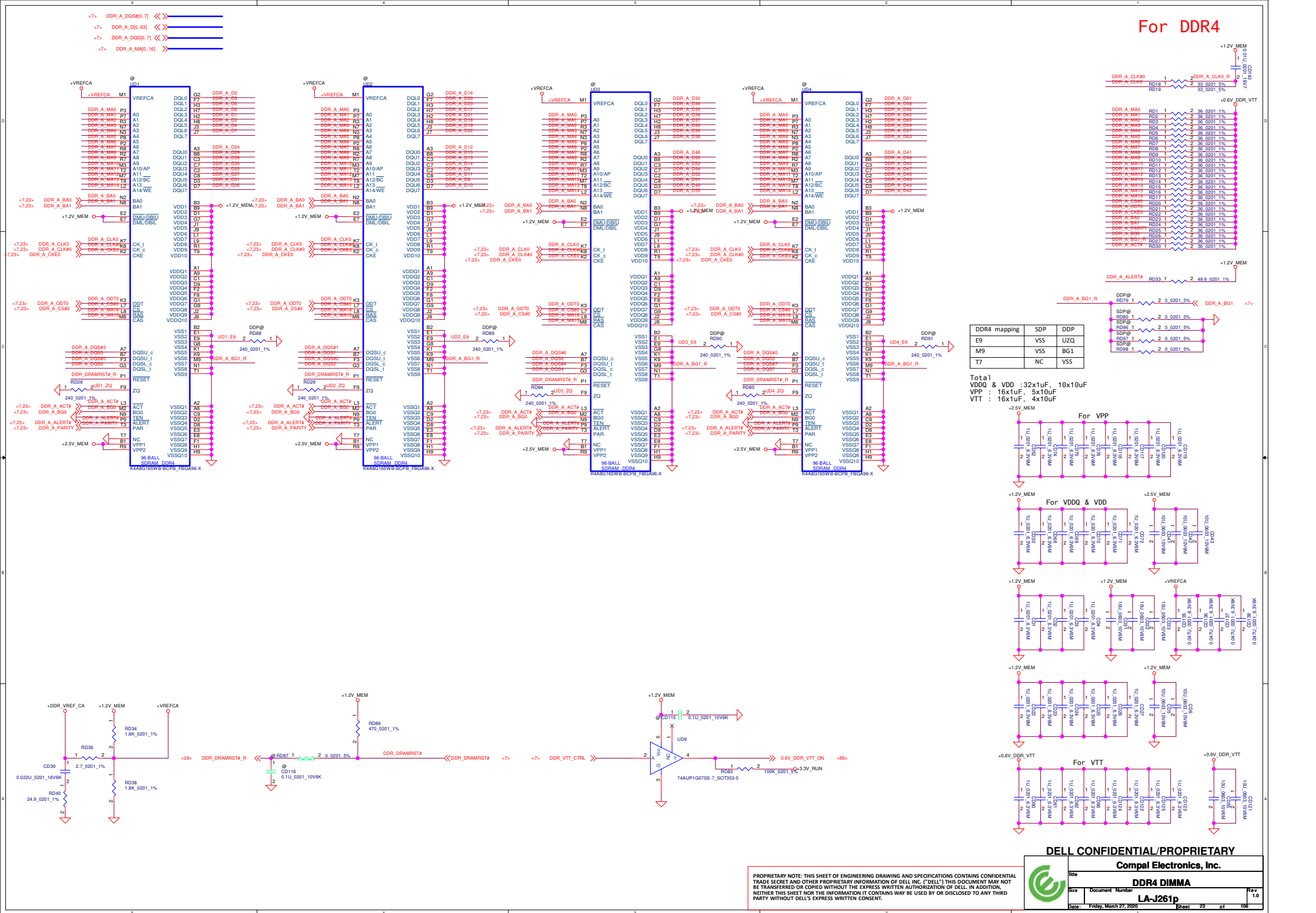
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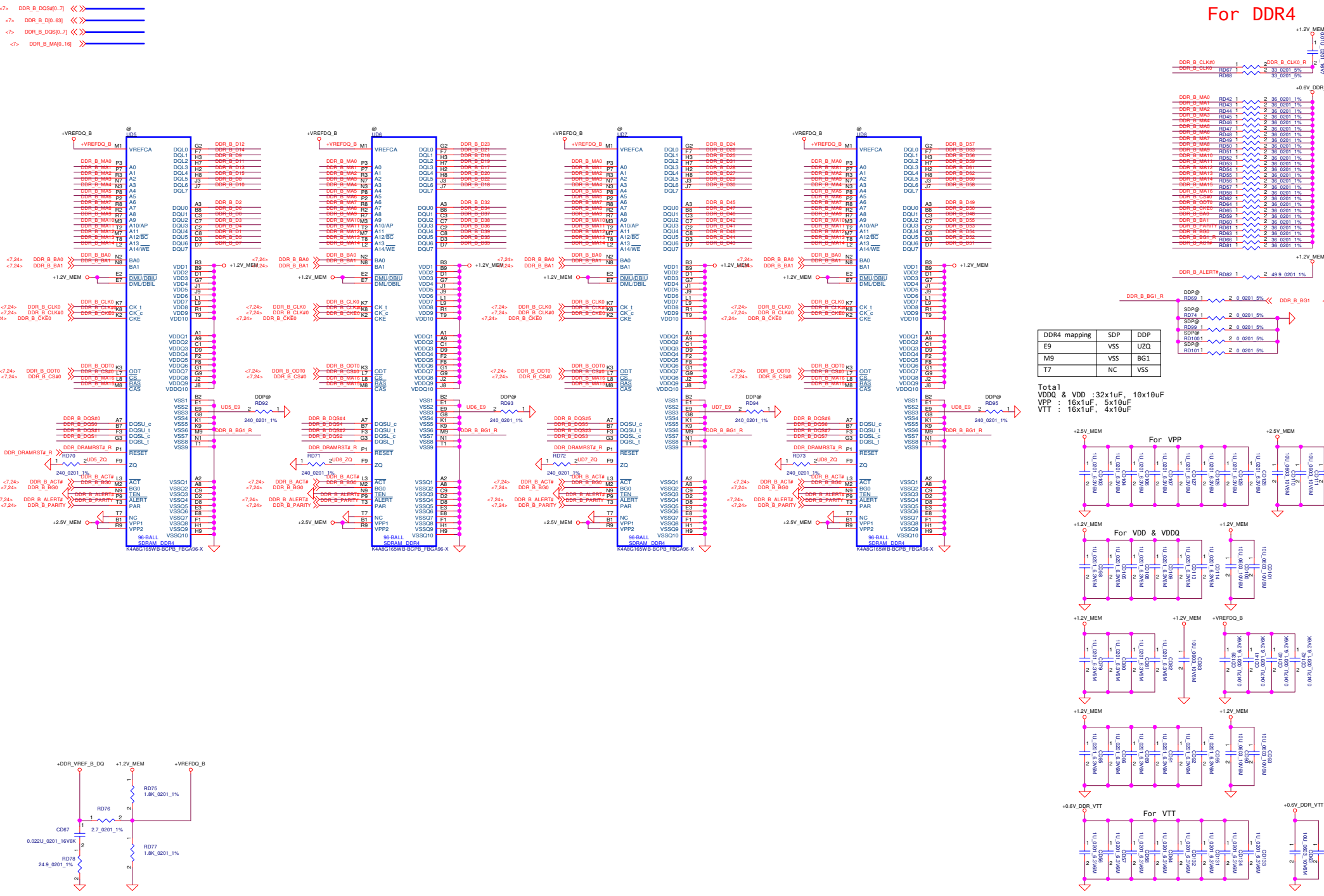
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For DDR4



# For DDR4



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DDR4 DIMMB

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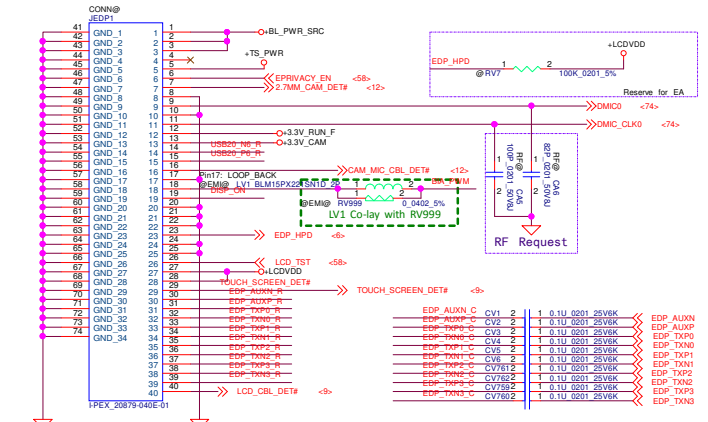
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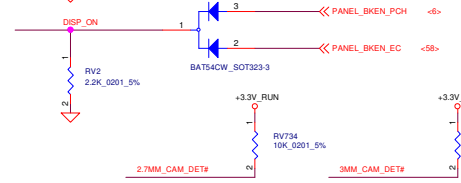
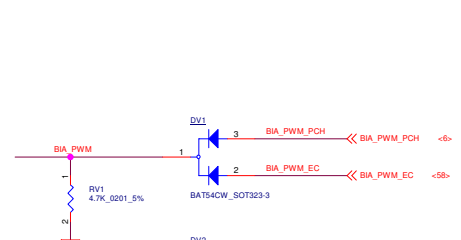
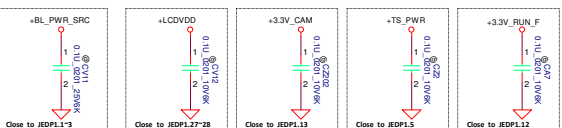
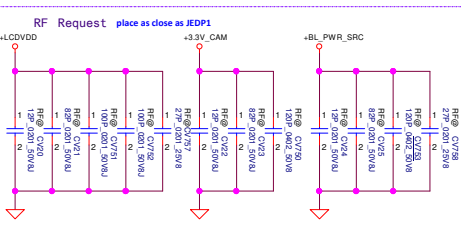
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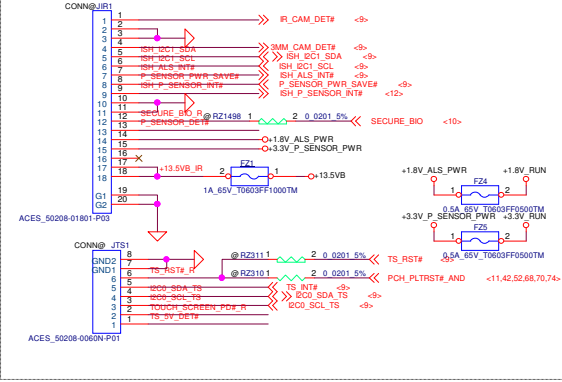


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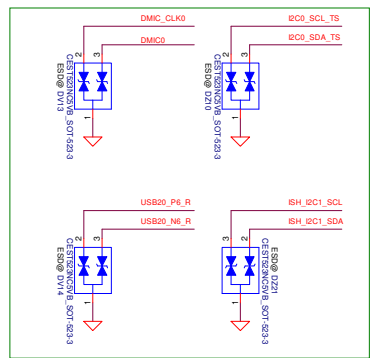
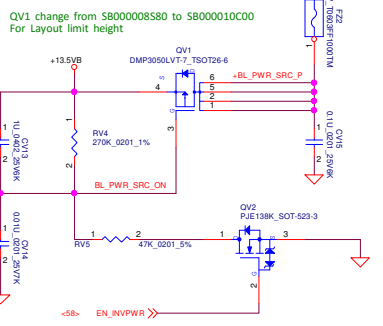


Camera Truth table	Mic Only	6mm Normal Camera	6mm IR Camera	3mm IR Camera	2.7mm HD Camera
GPP_G0(CAM_MIC_CBL_DET#)	H	L	L	L	L
GPP_D9(IR_CAM_DET#)	H	H	H	H	L
GPP_C20(3MM_CAM_DET#)	H	H	H	L	H
GPP_A16(2.7MM_CAM_DET#)	H	H	H	H	L
Antenna Location	Bottom	Top	Top	Bottom	Bottom

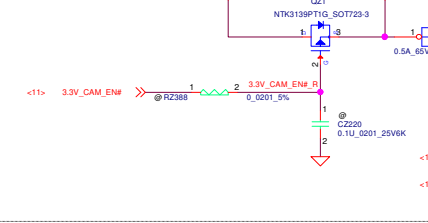
### TOUCH SCREEN & IR CAMERA connector



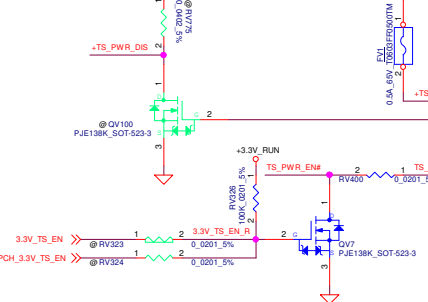
### Backlight POWER



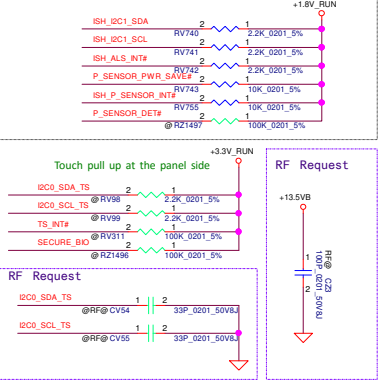
### WebCAM



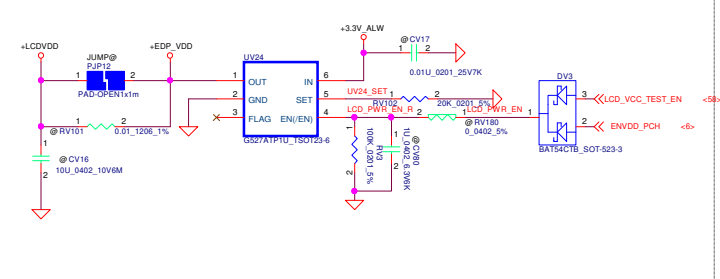
### For Touchscreen



### For 3mm IR CAM ALS & P-Sensor



### LCDVDD POWER



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**Compal Electronics, Inc.**

**eDP CONN & Touch screen**


**LA-J261p**

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DP

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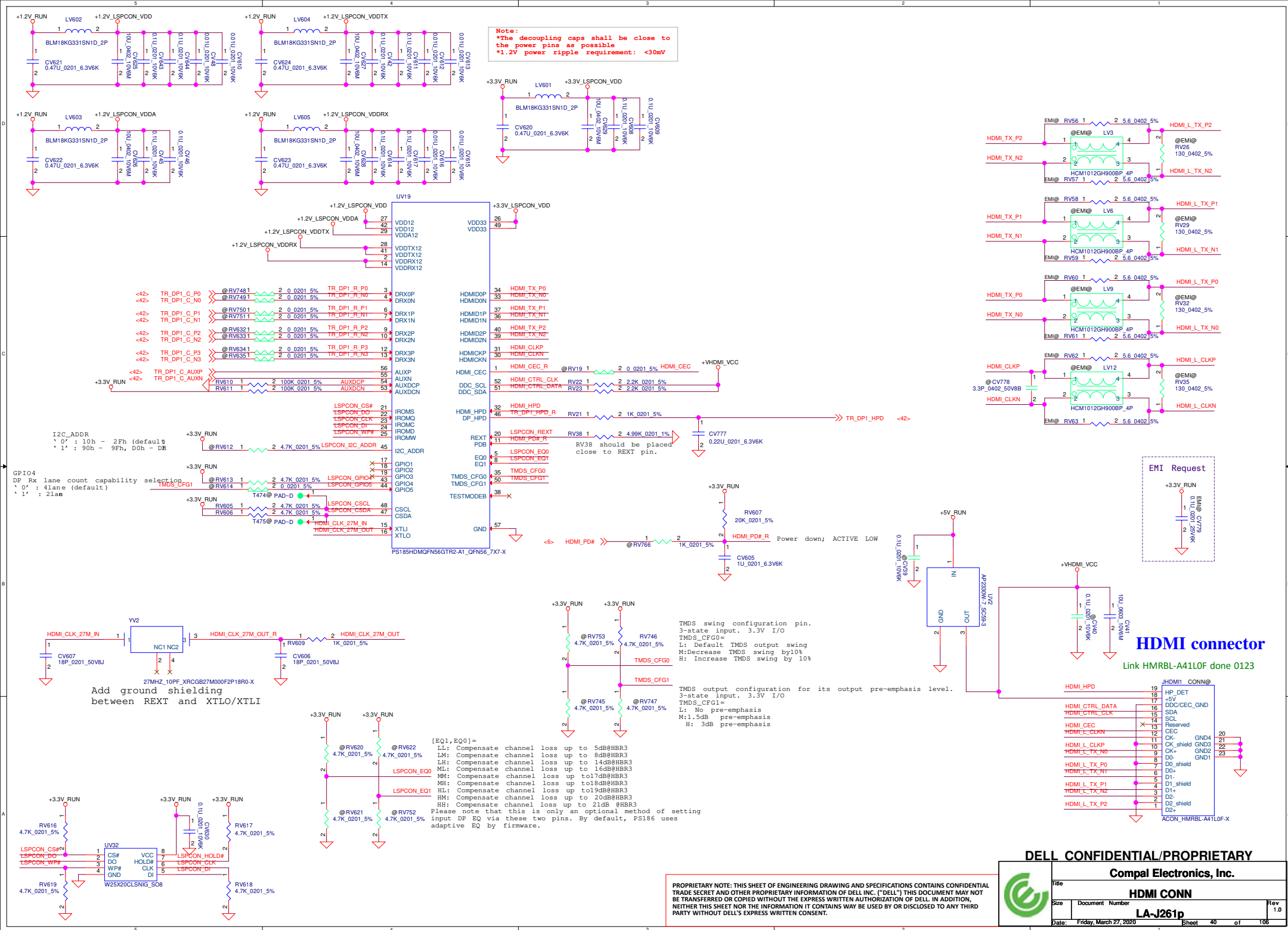
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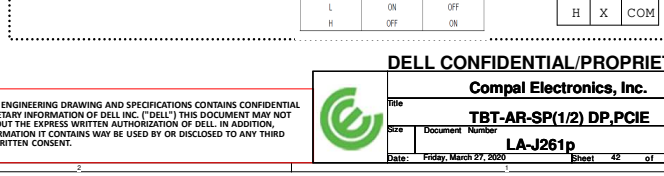
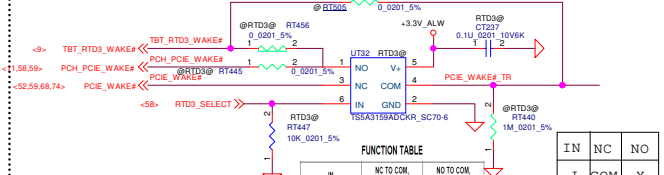
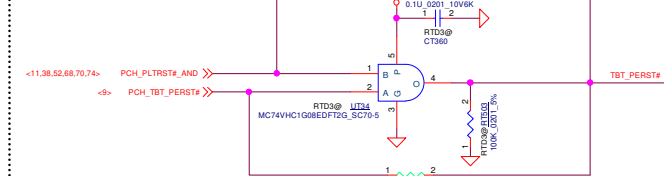
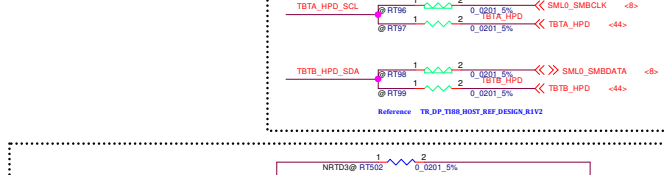
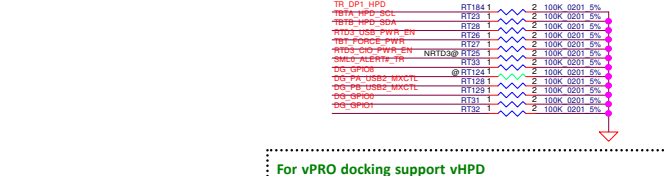
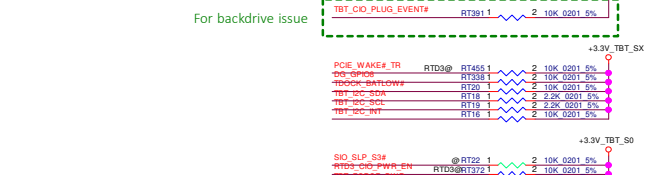
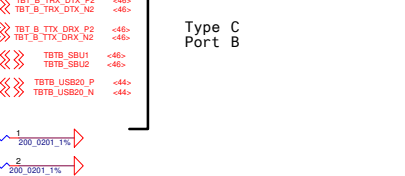
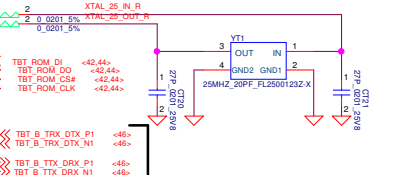
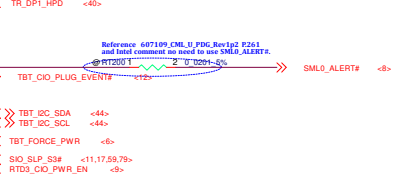
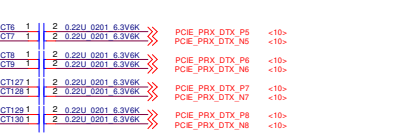
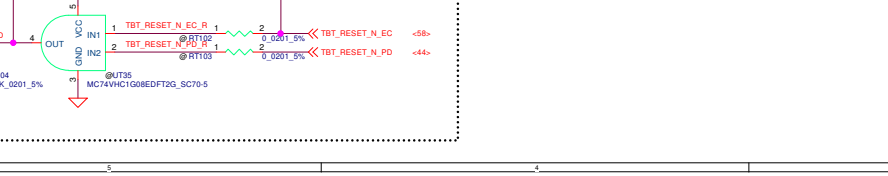
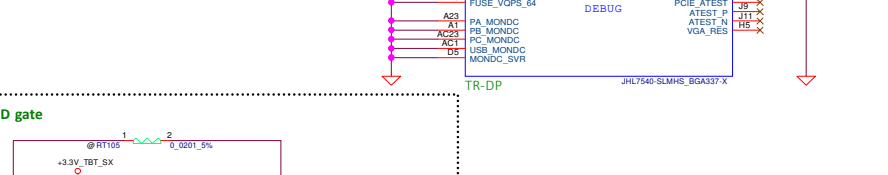
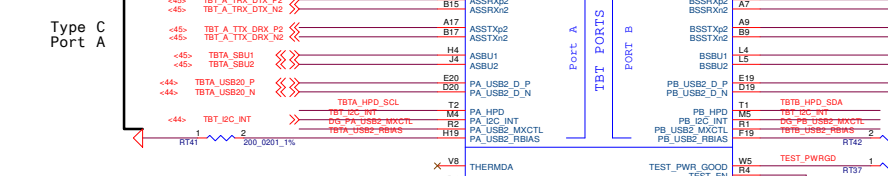
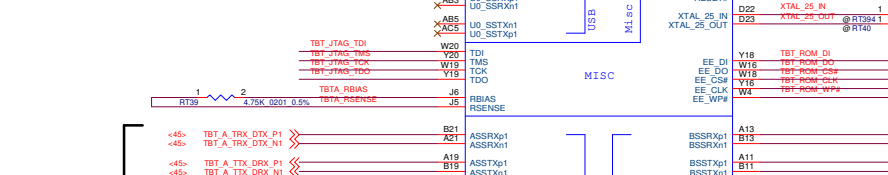
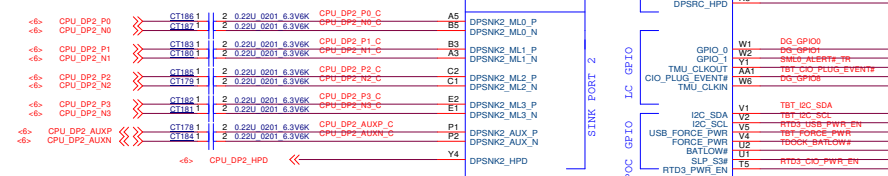
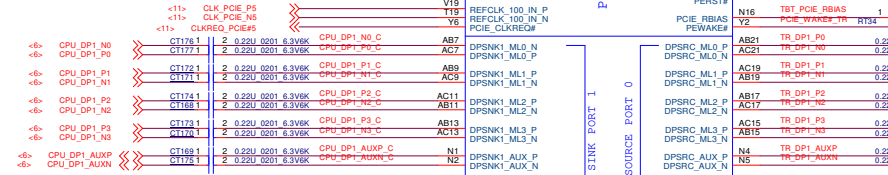
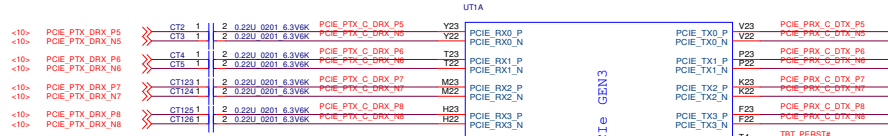
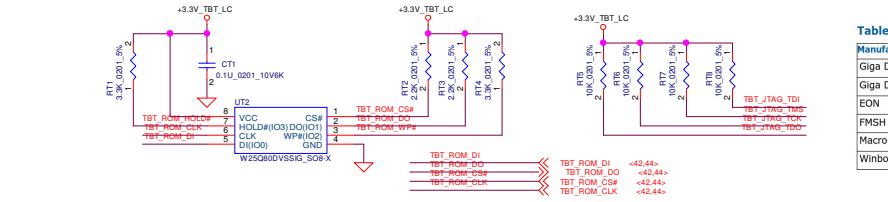
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# TR ROM choice need follow Intel approved list

Reference Titan Ridge DP 1.41 Datasheet  
Table 12. Supported types of Flash Memory

Manufacturer	Type	Volume, Mbit	Supply, V
Giga Device	GD25Q80C	8.0	2.7-3.6
Giga Device	GD25Q80CTIG	8.0	3.3
EON	EN25Q80B	8.0	2.7-3.6
FMSH	FM25Q08	8.0	2.7-3.6
Macronix	MX25L8006EM11	8.0 (150ml, 8-SOP)	2.7-3.6
Winbond	W25Q80DL	8.0	2.3-3.6



For backdrive issue

For vPRO docking support vHPD

TBT RTD3 Support

TBT Reset AND gate

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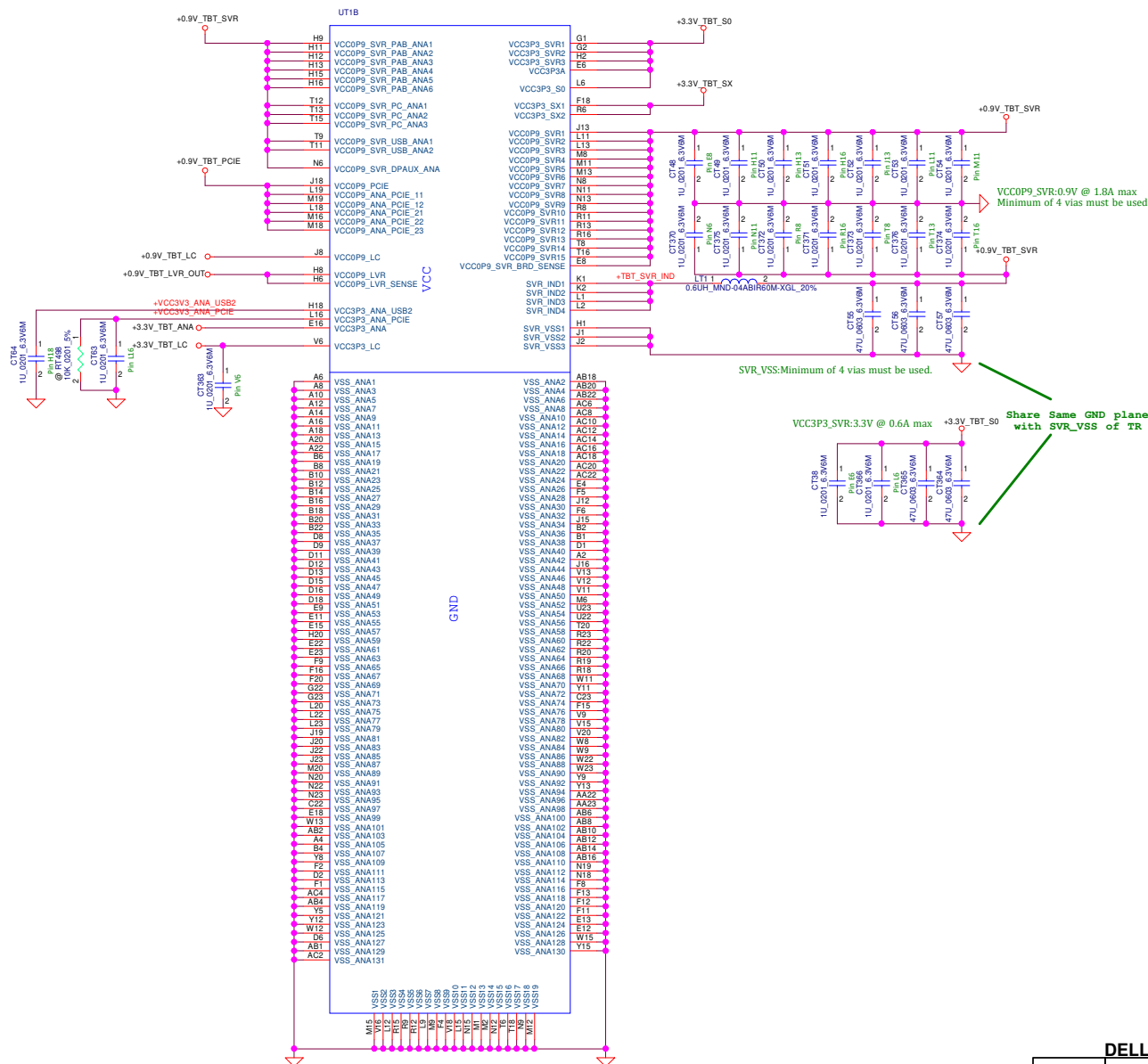
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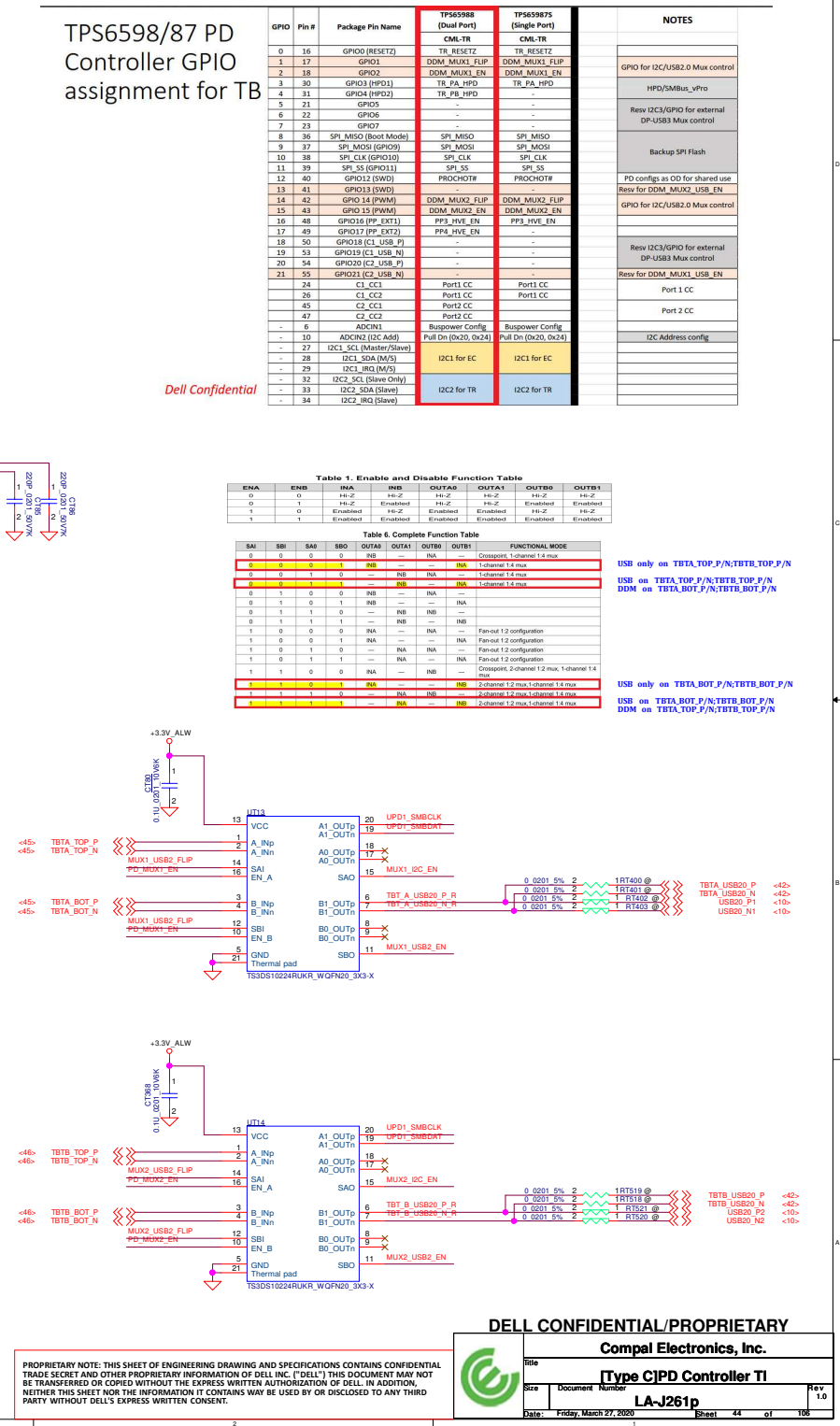
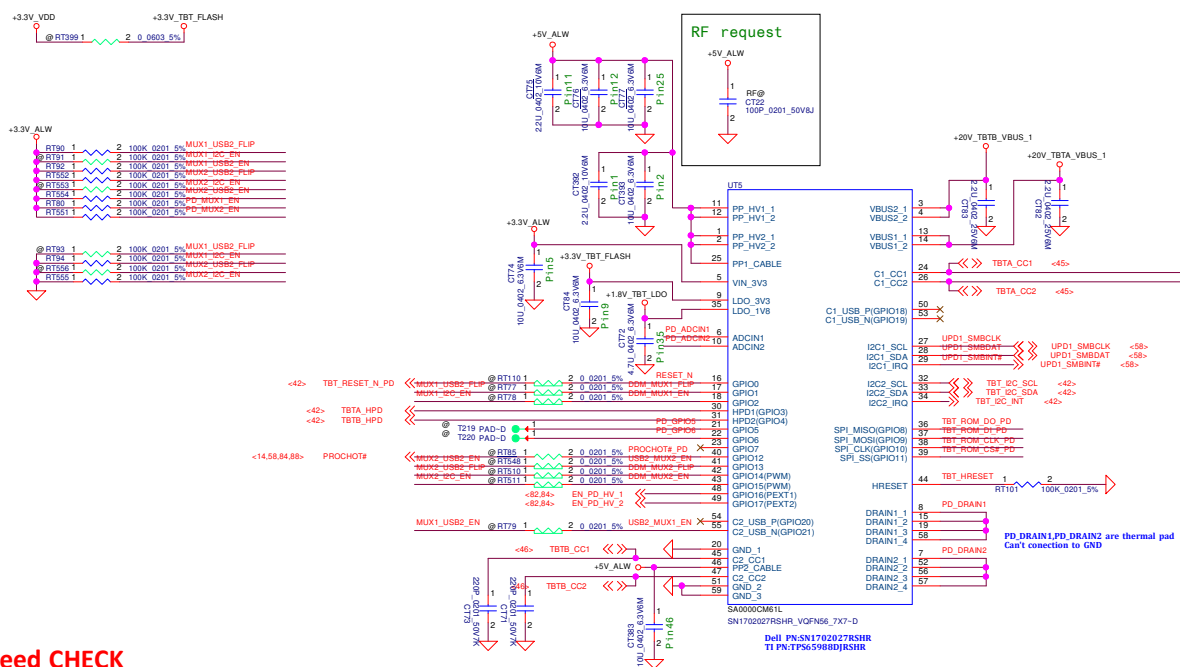


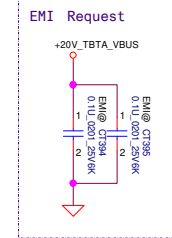
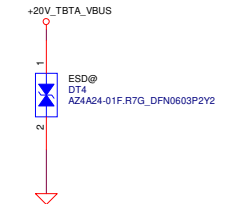
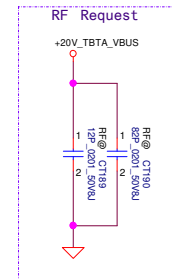
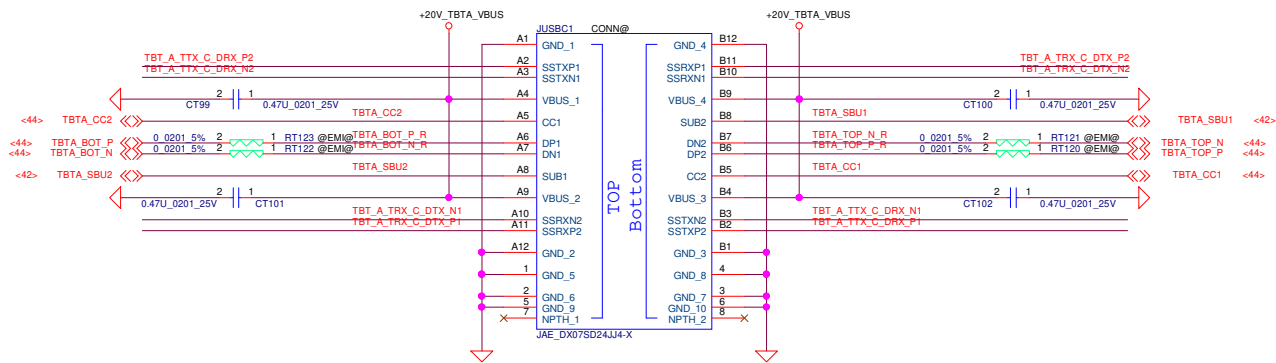
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	Title <b>TBT-AR-SP(2/2) VCC/VSS</b>			
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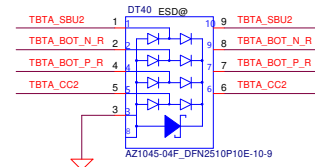
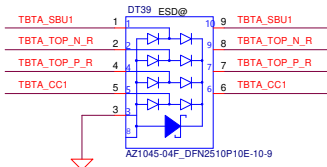
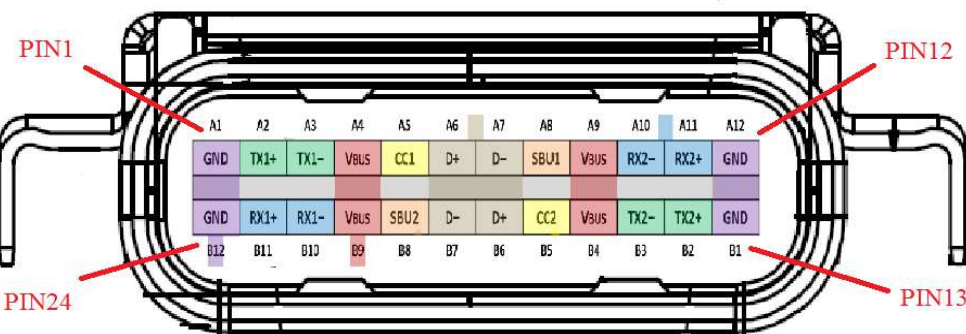
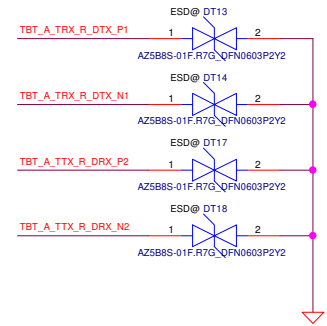
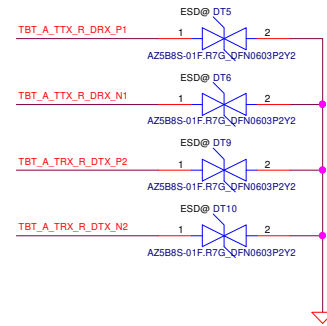
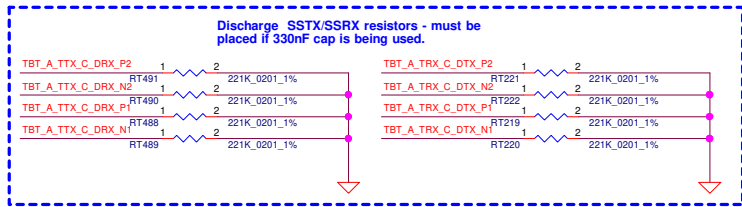
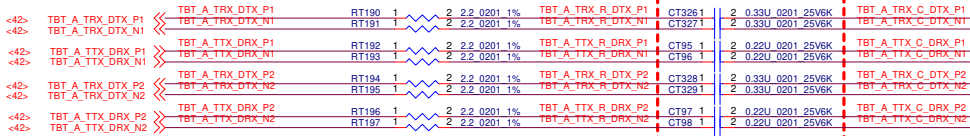
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Place holder for future VBUS-short fix (reduce current surge)

AC coupling is recommended for VBUS-short protection on SSRX lines. If not needed, place 0 Ohm resistor instead.



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USB 3.0 CONN TYPE C

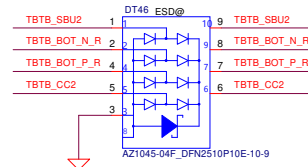
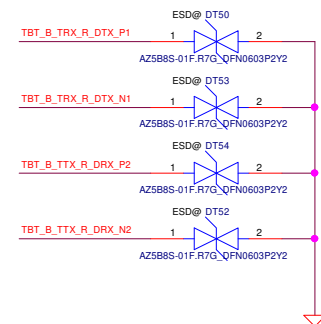
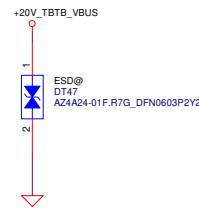
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Reserve for external PD power

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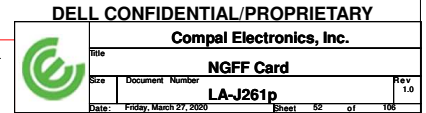
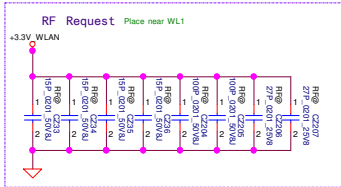
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**Compal Electronics, Inc.**

**USB/PCIE MUX HD3SS3212**

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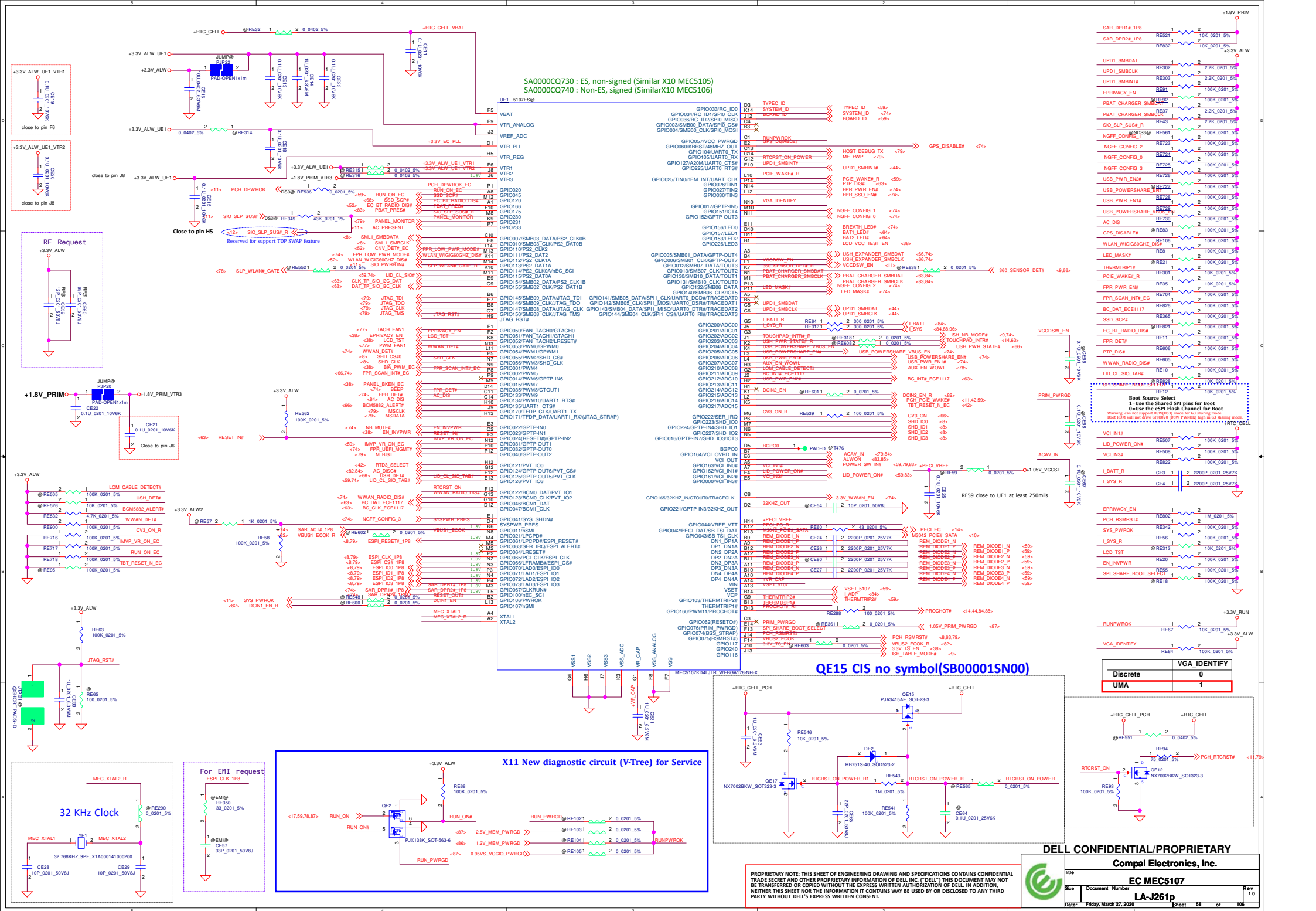
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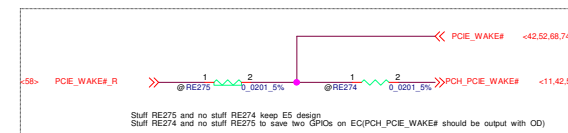
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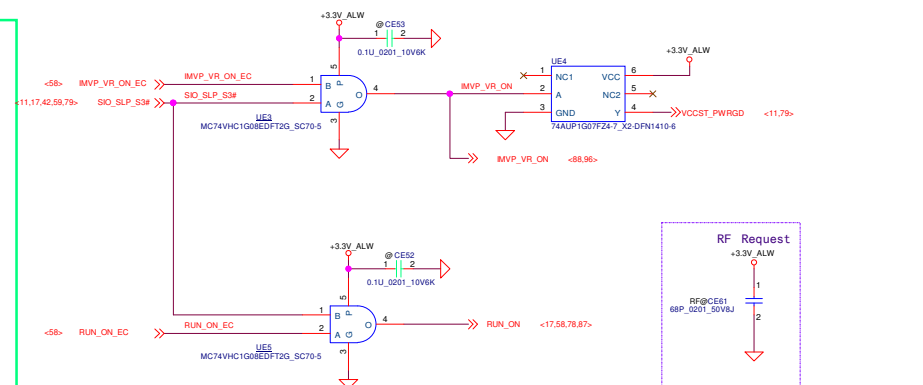
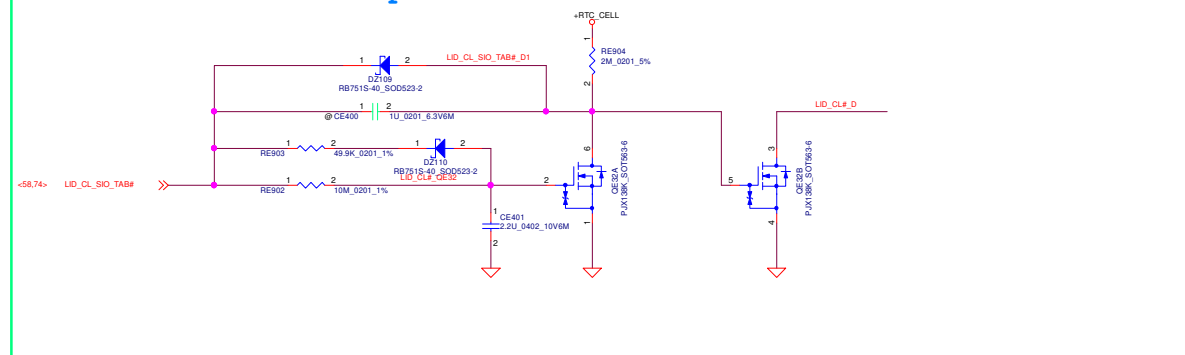
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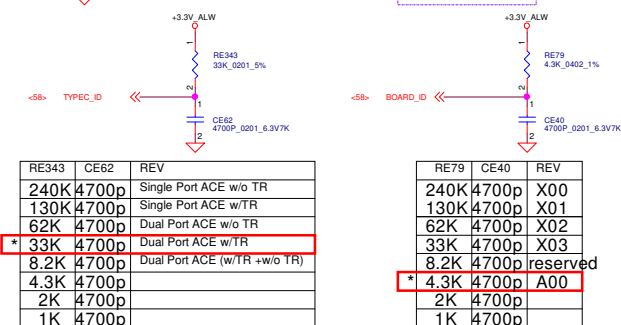
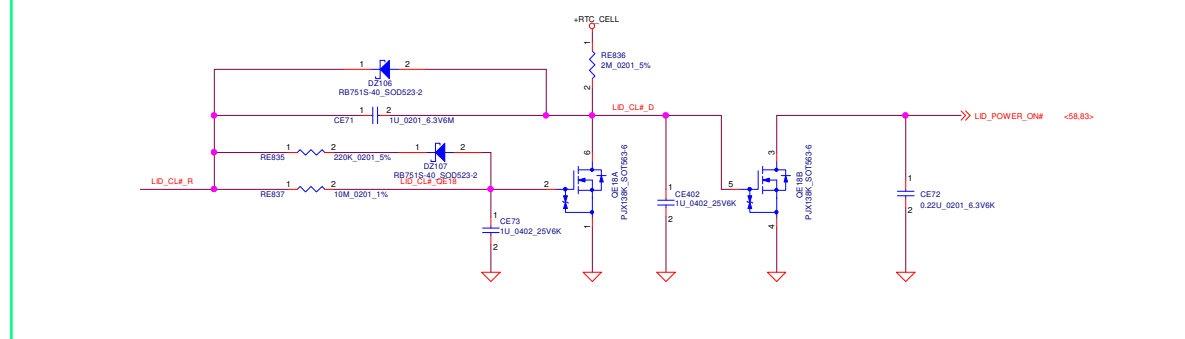




Fixed 360 casue auto power on



S5 LID OPEN POWER ON

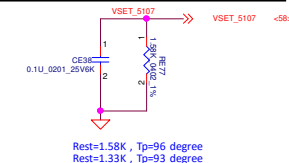


RE343	CE62	REV
240K	4700p	Single Port ACE w/o TR
130K	4700p	Single Port ACE w/TR
62K	4700p	Dual Port ACE w/o TR
* 33K	4700p	Dual Port ACE w/TR
8.2K	4700p	Dual Port ACE (w/TR +w/o TR)
4.3K	4700p	
2K	4700p	
1K	4700p	

	RE79	CE40	REV
	240K	4700p	X00
	130K	4700p	X01
	62K	4700p	X02
	33K	4700p	X03
	8.2K	4700p	reserved
*	4.3K	4700p	A00
	2K	4700p	
	1K	4700p	

TYPEC ID rise time is measured from 0%~63.2%

BOARD ID rise time is measured from 0%~63.2%

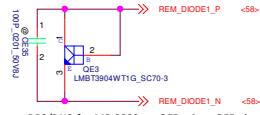


### Thermal diode mapping

5107 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	2280 SSD (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	Charger Choke (QE30)
DP4/DN4	CPU VR (QE6)

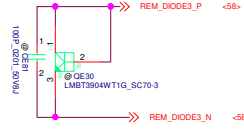
Place under CPU

Place CE35 close to the QE3 as possible



Place on PL701 charger choke  
Place C581 close to the Q520 as possible

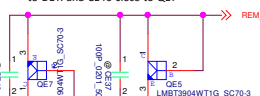
Place CE81 close to the QE30 as possible



DP2/DN2 for M2 2280 on QE5, place QE5 close to JNGFF3 and CE37 close to QE5

DN2a/DP2a for DDR on QE7, place QE7 close to DDR and CF46 close to QE7

DP4/DN4 for Skin on  
QE6, place QE6 close to  
Vcore VR choke.



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<b>Compal Electronics, Inc.</b>			
Title			
<b>MEC5107 support</b>			
Size	Document	Number	Re
		<b>LA-J261p</b>	
Date:	Friday, March 27, 2020		
	Sheet	59	of 108

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Title

Secure & Reset IC

Size

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LA-J261p

Date

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Title

LEDs (Controller)

Size

Document Number

LA-J261p

Date

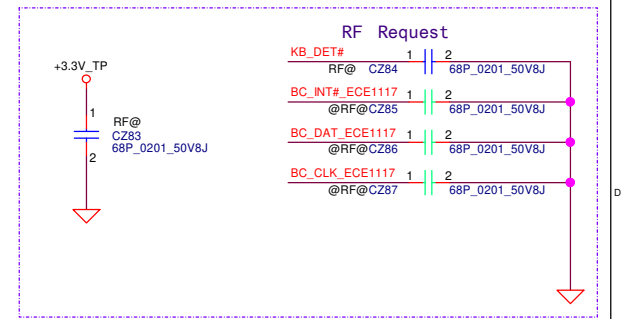
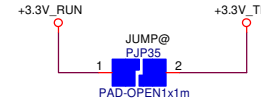
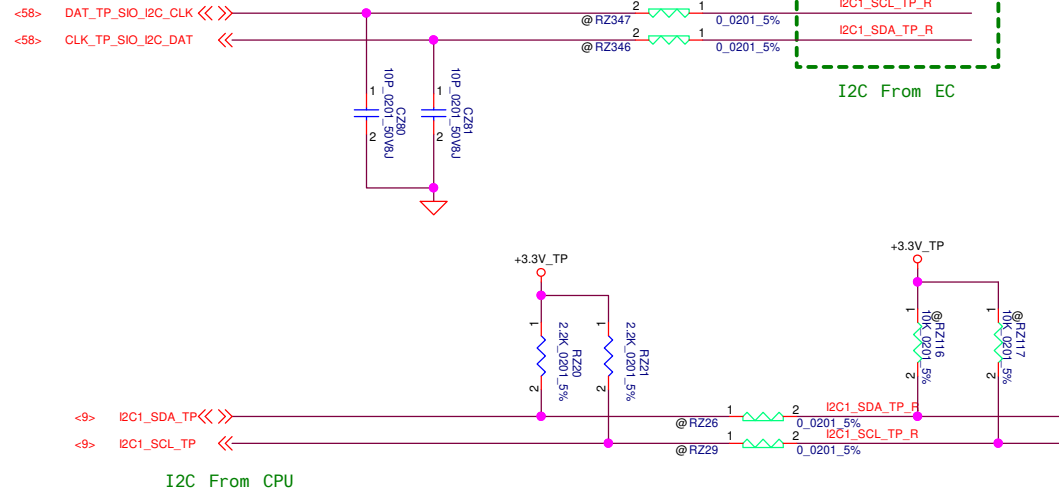
Friday, March 27, 2020

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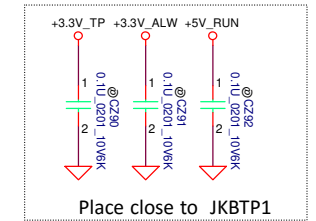
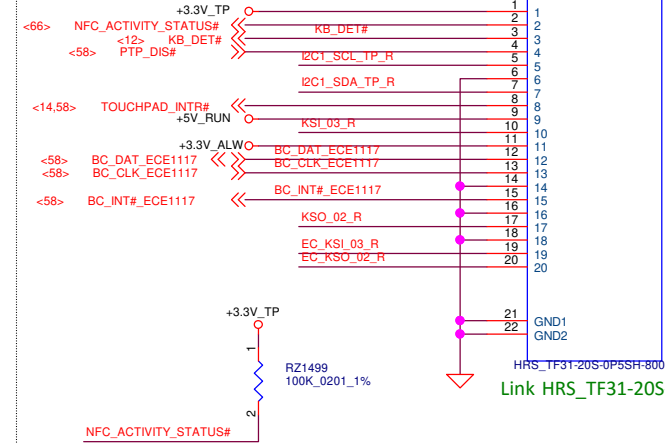
Rev

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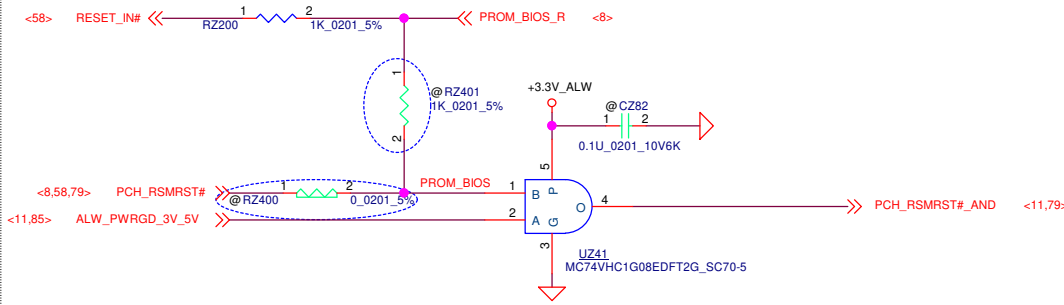
# Touch Pad



## Keyboard



## RSMRST circuit



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Keyboard

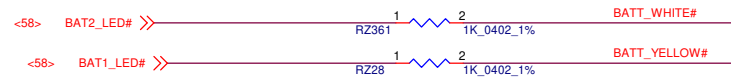
LA-J261p

Size Document Number Rev 1.0  
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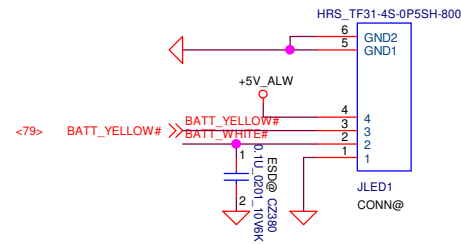
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## Battery LED



## LED board CONN



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Title

Reserve for KB/TP/LED/LID

Size

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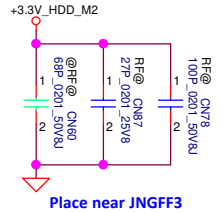
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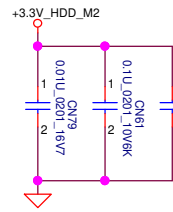
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Compal Electronics, Inc.			
Title			
HDD/ODD/FFS Connector			
Size	Document Number		Rev
	LA-J261p		1.0
Date:	Friday, March 27, 2020		Sheet 67 of 106

# Add Power Decoupling for support Intel Teton Glacier

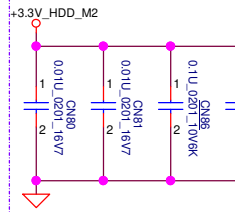
## RF Request



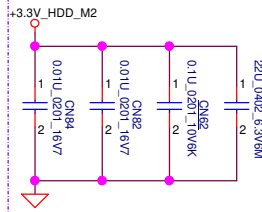
## Place close JNGFF3 pin 12,14,16,18



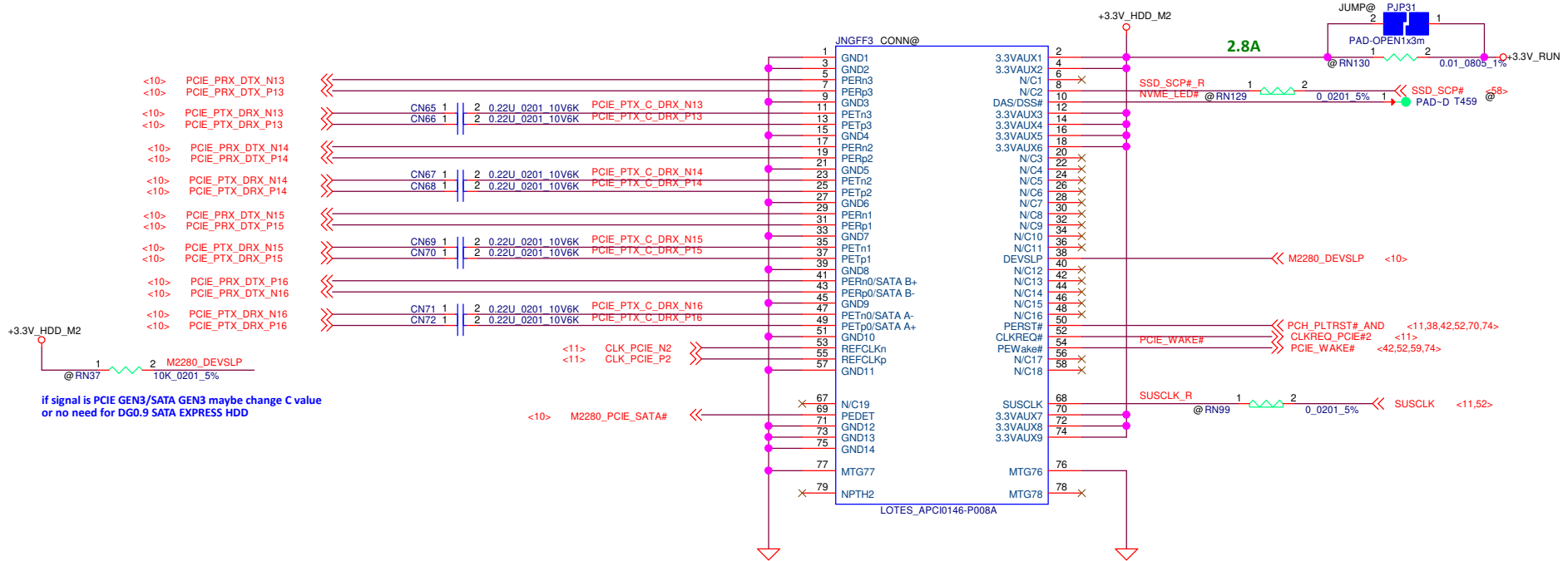
## Place close JNGFF3 pin 2,4



## Place close JNGFF3 pin 70,72,74



## 2280 SSD NGFF slot C Key M



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M2 2280 Socket

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Title

eMMC / UFS

Size

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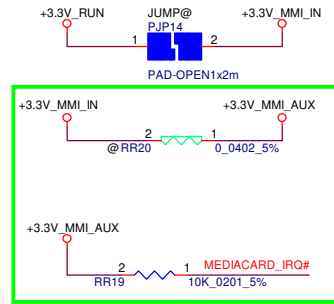
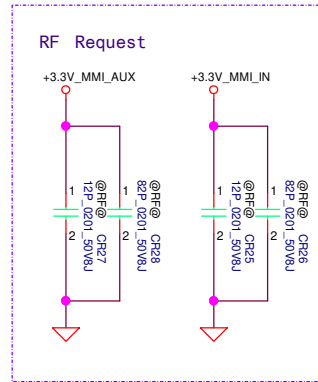
Friday, March 27, 2020

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# For PCIE Interface



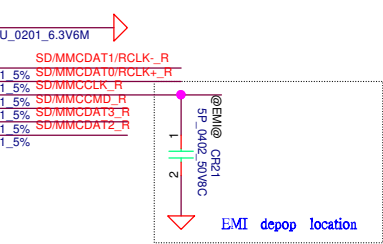
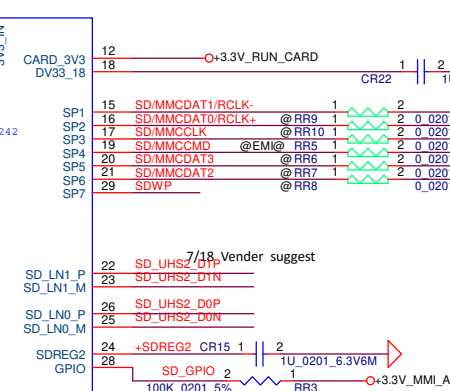
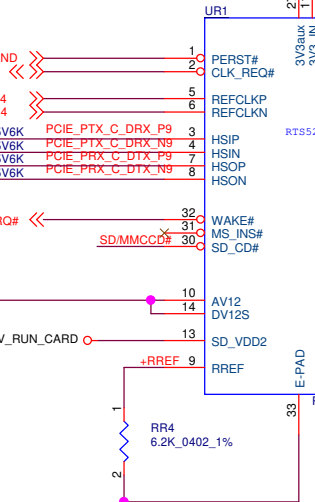
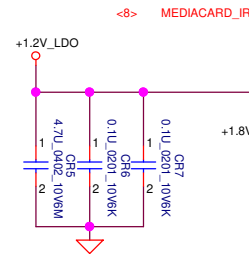
support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/off 3V3AUX)

7/18 Vender suggest.

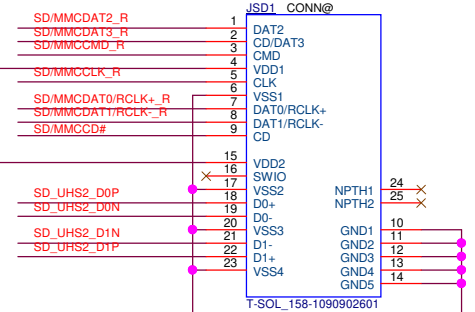
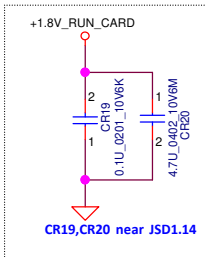
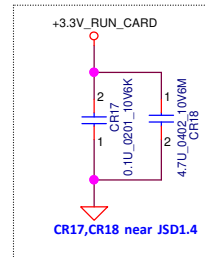
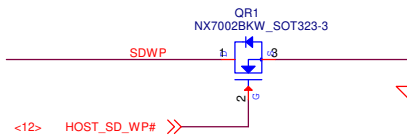
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<10> PCIE\_PT\_X\_DTX\_N9

<11> CLK\_PCIE\_P4  
<11> CLK\_PCIE\_N4

<8> MEDIACARD\_IRQ#



HOST_SD_WP#	SDWP	STATUS
High	Low	Write Enable
Low	High	Write Protect(FW LOCK)



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Card Reader RTS5242

LA-J261p

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Size	Document Number		Rev
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Date:	Friday, March 27, 2020		Sheet 71 of 106



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TitleJUSB2

SizeDocument NumberLA-J261pRev1.0

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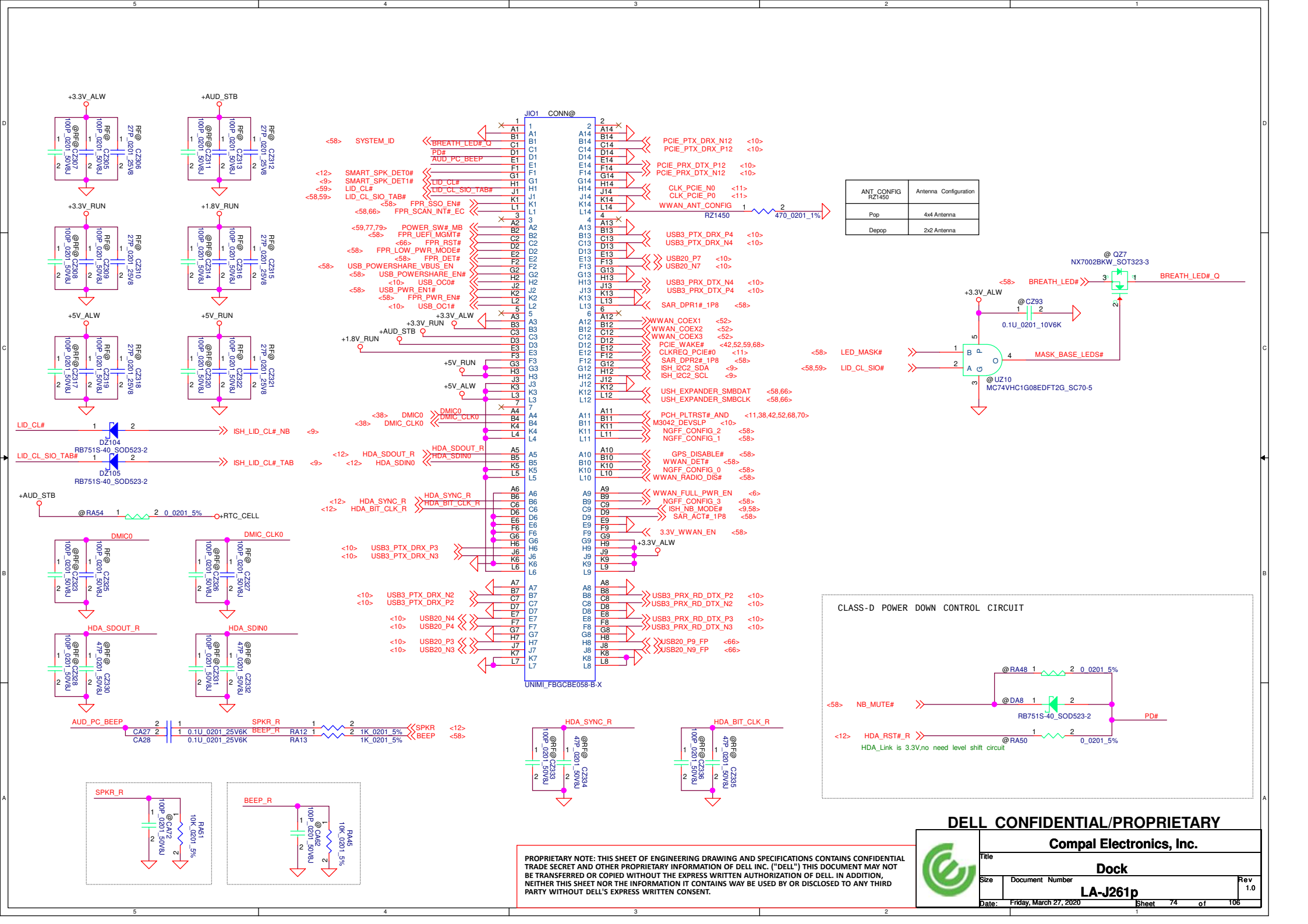
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Title **USB2/USB3 DB**

Size	Document Number	Rev
	<b>LA-J261p</b>	<b>1.0</b>

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Title			
Reserve for USB			
Size	Document Number		Rev
	LA-J261p		1.0
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Title

Reserve for USB

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LA-J261p

Date

Friday, March 27, 2020

Sheet

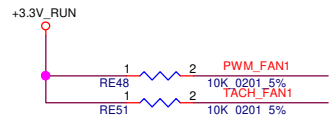
76

of

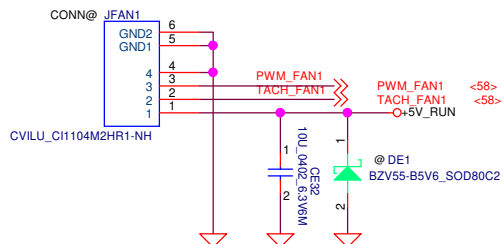
106

Rev

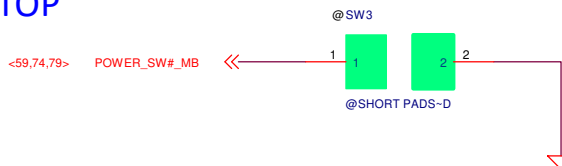
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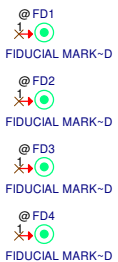
Link 50271-0040N-001 done 0123



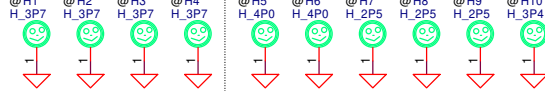
## POWER & INSTANT ON SWITCH TOP



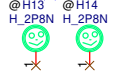
## Fiducial Mark



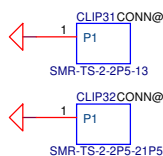
## CPU



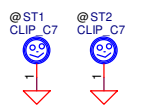
## FBEAM



## Gasket



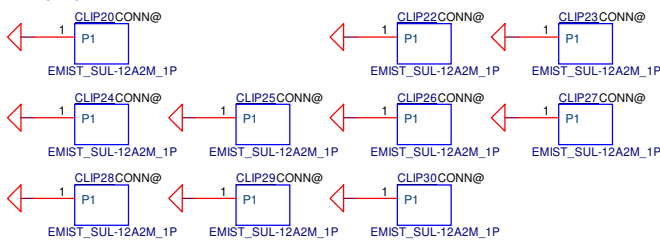
## EDP



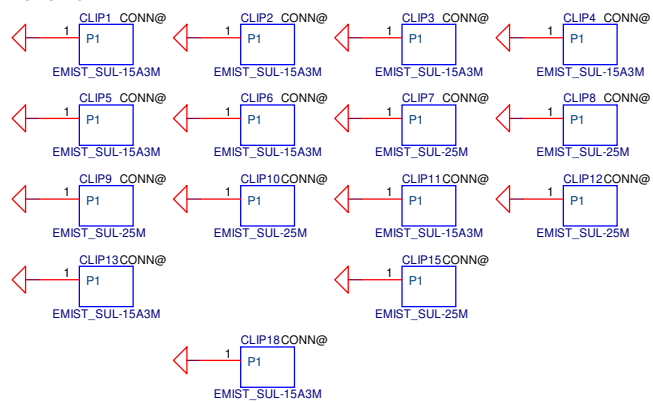
## SSD



## DDR CLIPS



## BOT CLIPS



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PWRBTN, PAD, ME, FAN

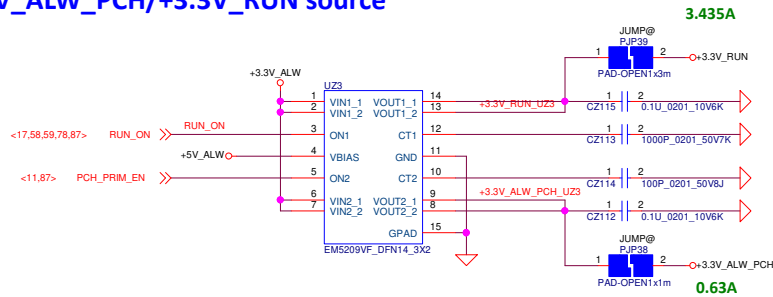
LA-J261p

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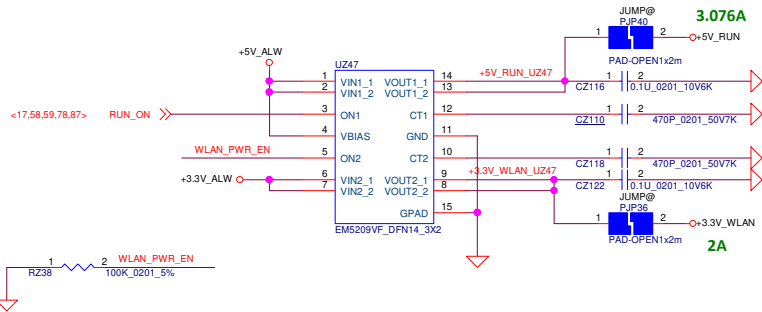
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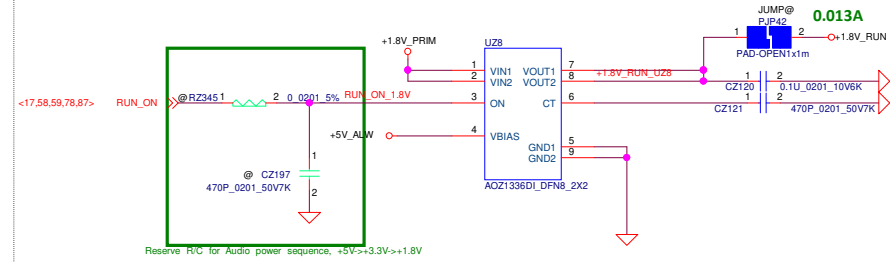
### +3.3V\_ALW\_PCH/+3.3V\_RUN source



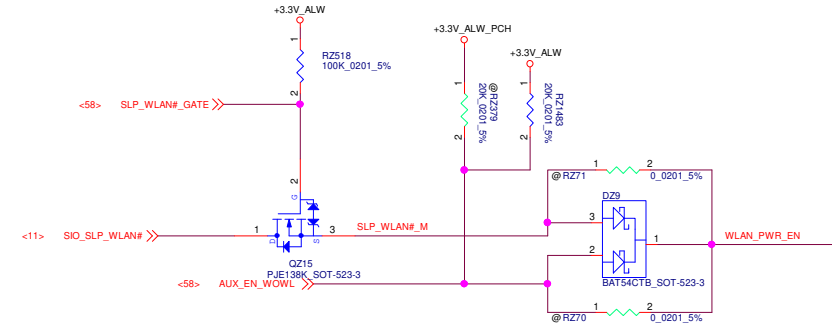
### +5V\_RUN/+3.3V\_WLAN source



### +1.8V\_RUN source

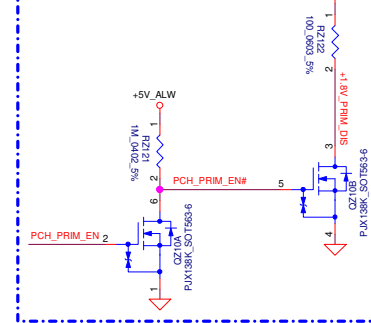


EC request to reserve OR gate for WLAN power enable



### +1.8V\_PRIM discharge circuit

Need to be close to the source (PJP502)



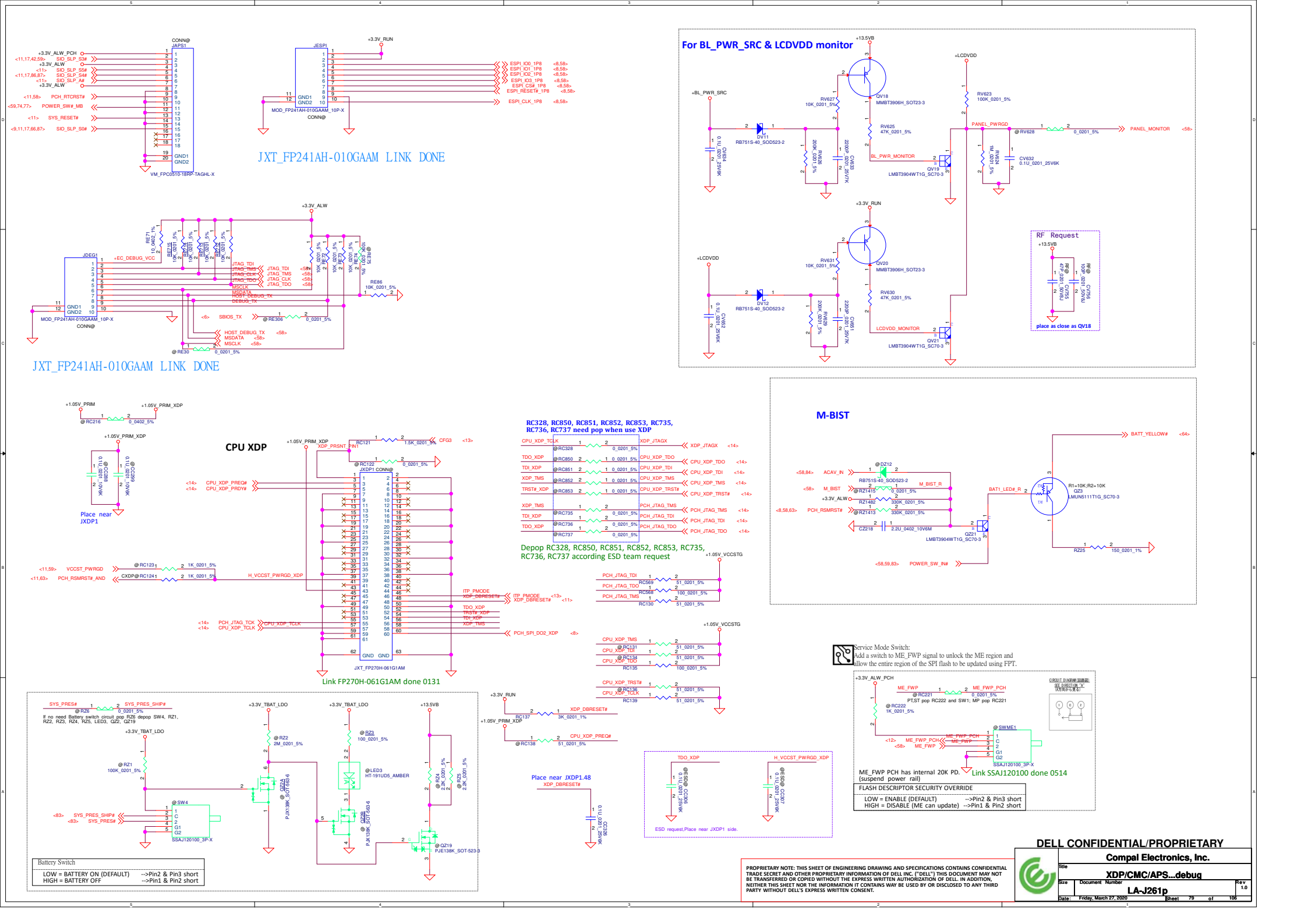
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**Google Debug & INAs**


**LA-J261p**

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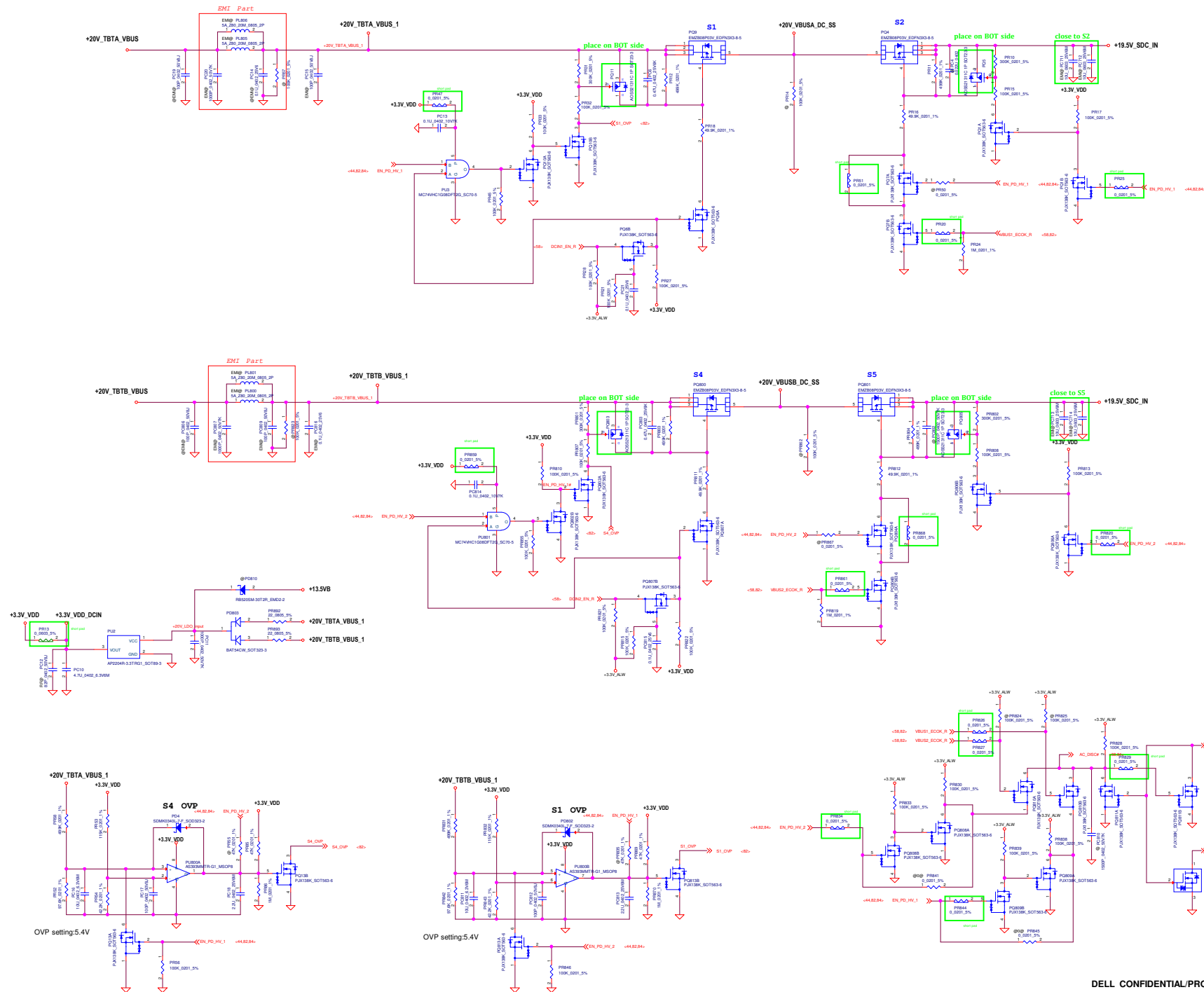


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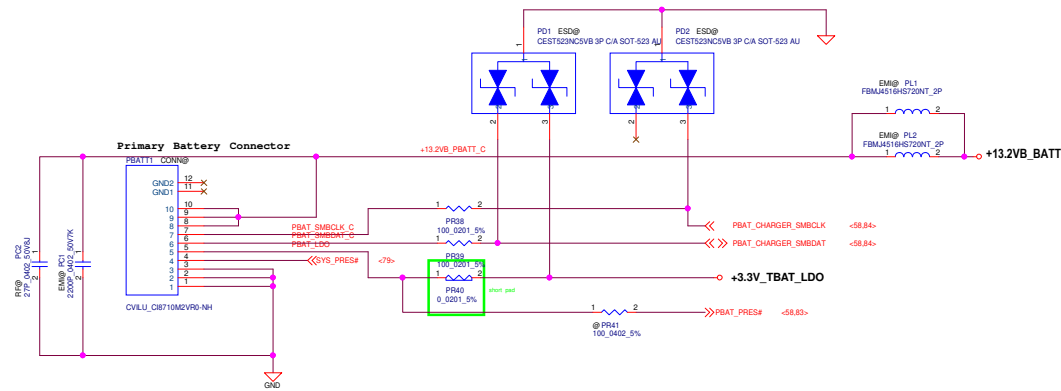


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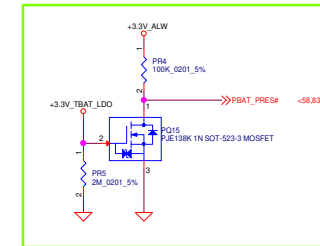
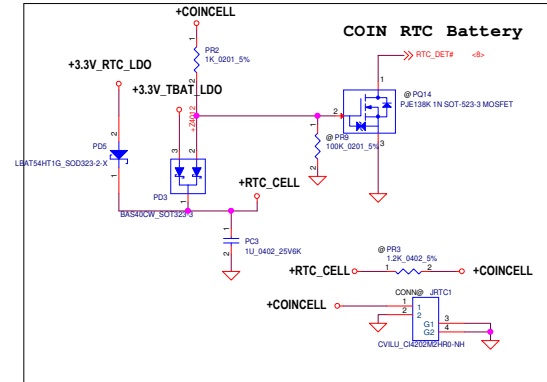
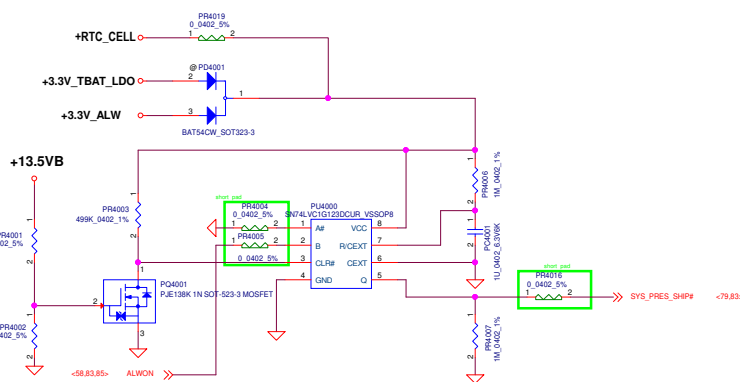
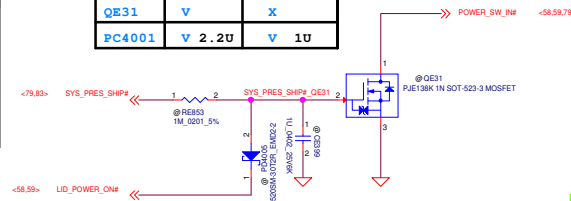


Note: new ASM support circuit

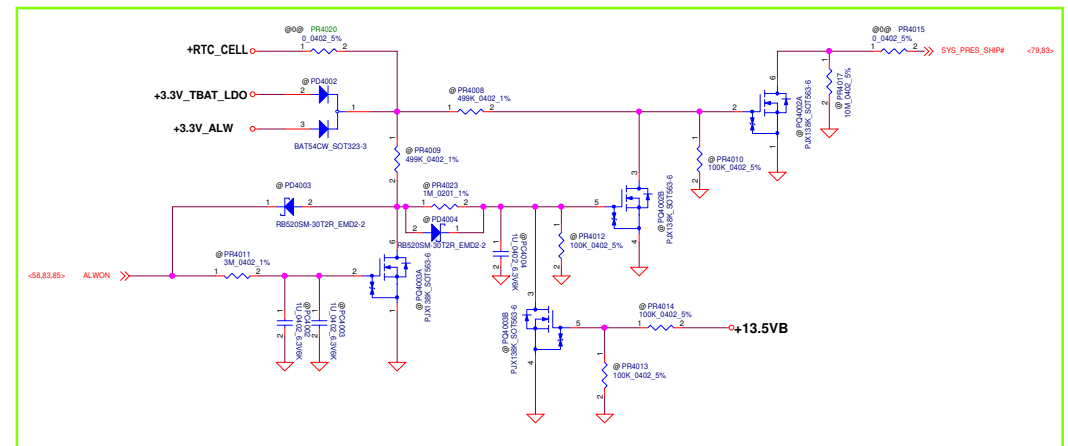
FUNCTION TABLE			
INPUTS			OUTPUTS
CLR	A	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	□
H	↓	H	□
↑	L	H	□

Location	pop	depop
RE853	V	X
PD4005	V	X
CE399	V	X
QE31	V	X
PC4001	V 2.2U	V 1U

Storage mode wake up circuit



Add for selection



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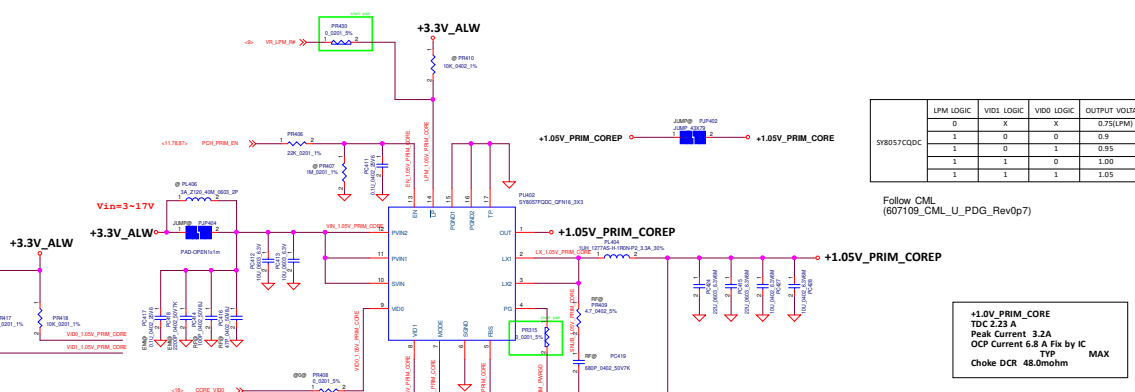
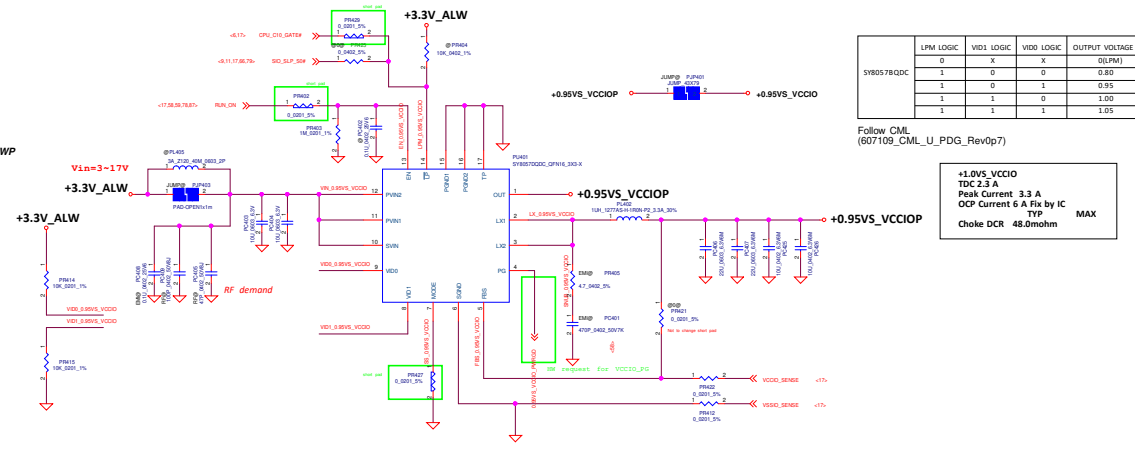
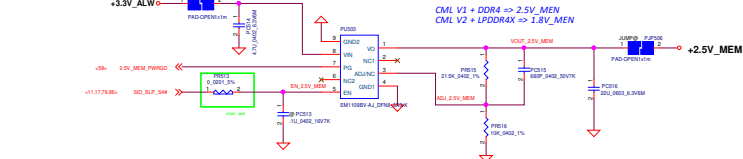
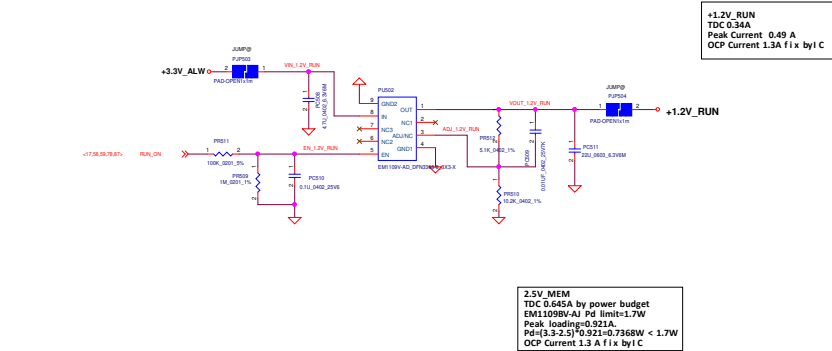
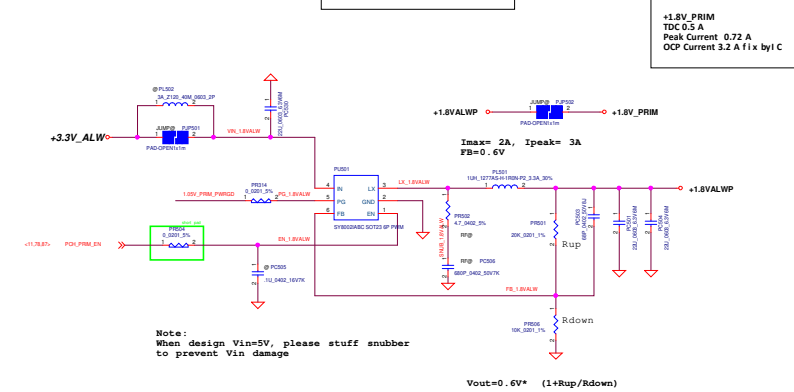
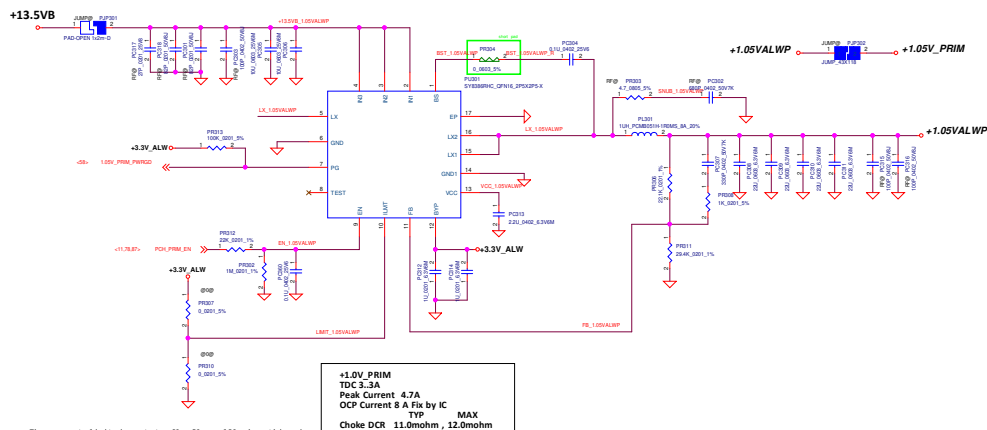
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LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
0	X	X	0.95V
1	0	0	0.95
1	1	0	1.00
1	1	1	1.05

Follow CML  
(607109\_CML\_U\_PDG\_Rev0p7)

LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
0	X	X	0.75V(LPM)
1	0	0	0.9
1	0	1	0.95
1	1	0	1.00
1	1	1	1.05

Follow CML  
(607109\_CML\_U\_PDG\_Rev0p7)

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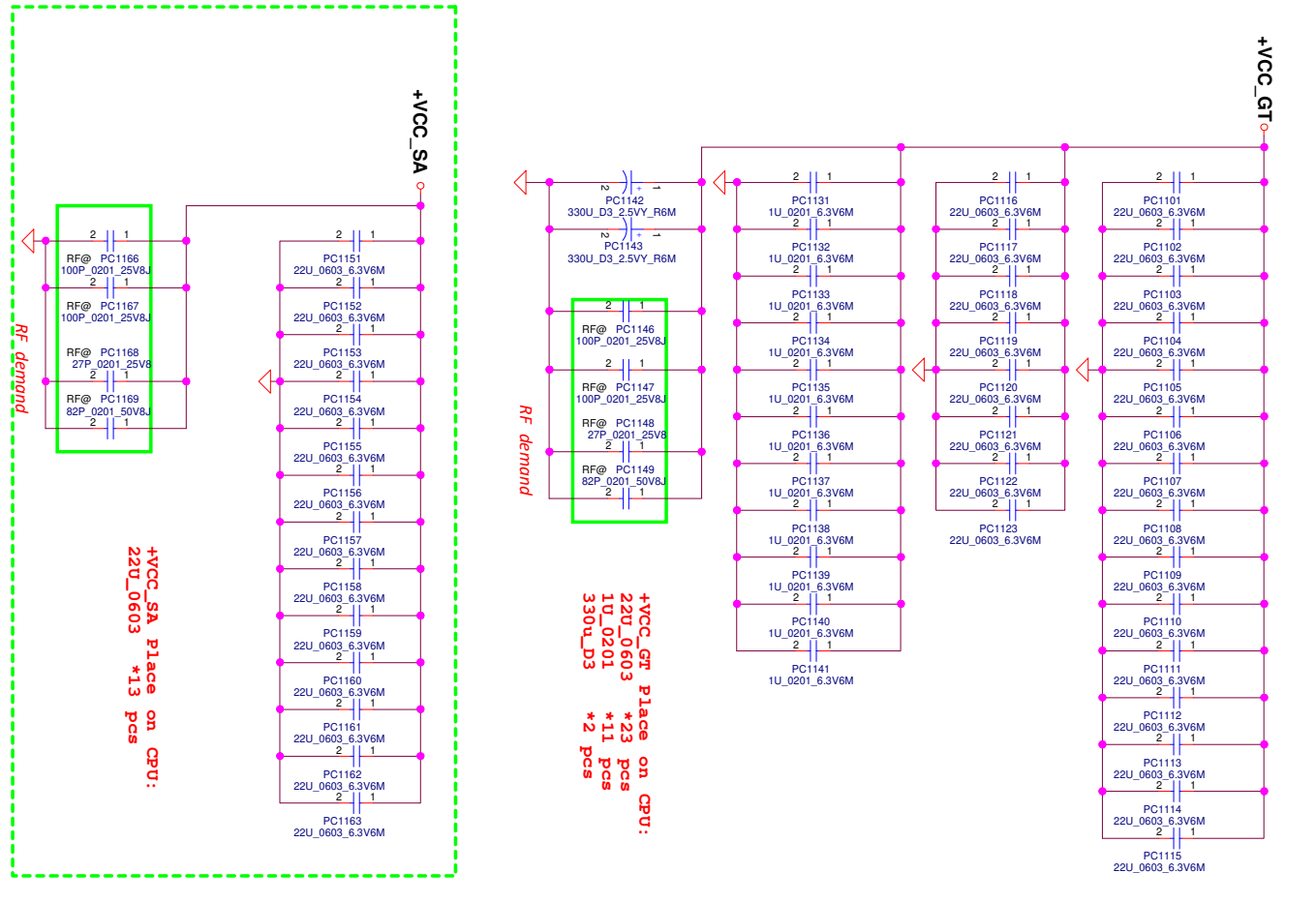
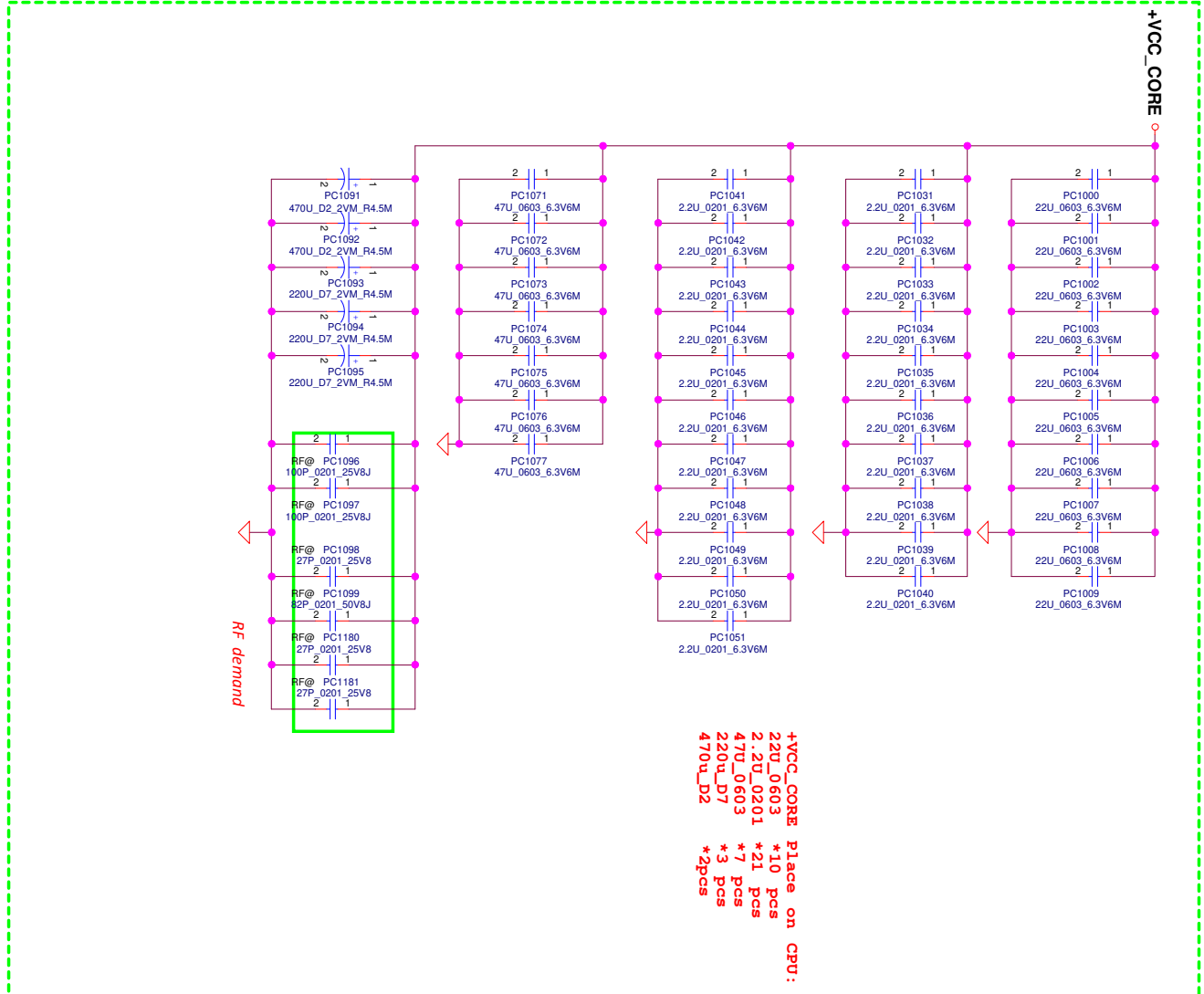
Compal Electronics, Inc.			
LA-1261P	LA-1261P	LA-1261P	LA-1261P
LA-1261P	LA-1261P	LA-1261P	LA-1261P
LA-1261P	LA-1261P	LA-1261P	LA-1261P

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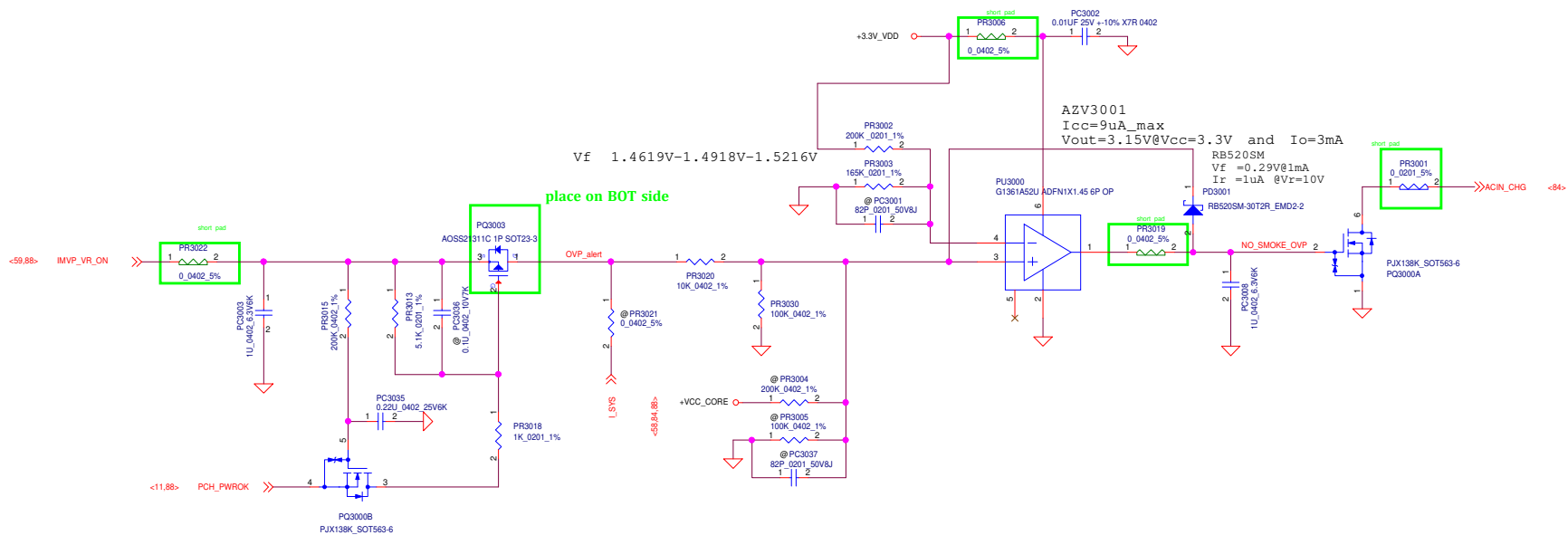
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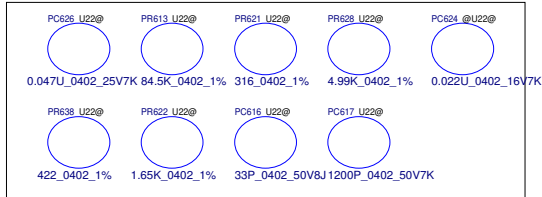
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## U22



Location	U42	[2phase]	U62	[2phase]
PC626	V	0.1U	V	0.1U
PR613	V	97.6K	V	97.6K
PR621	V	316	V	316
PR628	V	4.99K	V	4.99K
PR638	V	523	V	523
PR622	V	2.49K	V	2.49K
PC616	V	68P	V	68P
PC617	V	1200P	V	1200P
PC624	V	0.022U	V	0.022U

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## WLAN option AX201



## EC option



SA0000CQ740 : Non-ES, signed (SimilarX10 MEC5106)

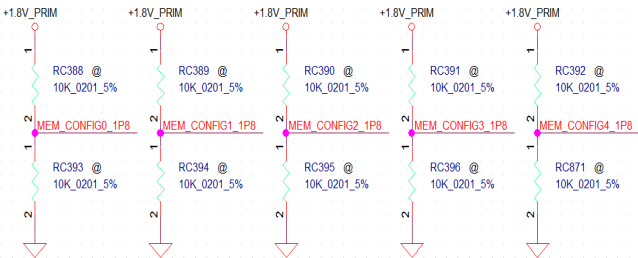
## WLAN option AX201(N)



## DRAM SDP E9 option



## DRAM Option Detail at Page 103



## X76

## DRAM Option

## Micron 4GB/2666(Channel A only)



X7688431L03

## Micron 4GB/2666(Channel A only)



## Micron 8GB/2666



X7688431L06

## Micron 8GB/2666



X7688431L09

## Micron 16GB/2666



## Micron 16GB/2666



## Micron 32GB/2666



X7688431L02

## Hynix 4GB/2666(Channel A only)



X7688431L05

## Hynix 8GB/2666



X7688431L08

## Hynix 16GB/2666



## Hynix 32GB/2666



X7688431L01

## Samsung 4GB/2666(Channel A only)



X7688431L04

## Samsung 8GB/2666



X7688431L07

## Samsung 16GB/2666



X7688431L10

## Samsung 32GB/2666



## DRAM Config Option

(Resistor pop location)

MEM_CONFIG0	MEM_CONFIG1	MEM_CONFIG2	MEM_CONFIG3	MEM_CONFIG4
RC393 M4G@ SD043100280	RC394 M4G@ SD043100280	RC395 M4G@ SD043100280	RC396 M4G@ SD043100280	RC392 M4G@ SD043100280
RC393 M4GN@ SD043100280	RC394 M4GN@ SD043100280	RC395 M4GN@ SD043100280	RC391 M4GN@ SD043100280	RC392 M4GN@ SD043100280
RC393 M8G@ SD043100280	RC394 M8G@ SD043100280	RC390 M8G@ SD043100280	RC396 M8G@ SD043100280	RC392 M8G@ SD043100280
RC393 M8GN@ SD043100280	RC394 M8GN@ SD043100280	RC390 M8GN@ SD043100280	RC391 M8GN@ SD043100280	RC392 M8GN@ SD043100280
RC393 M16G@ SD043100280	RC389 M16G@ SD043100280	RC395 M16G@ SD043100280	RC396 M16G@ SD043100280	RC392 M16G@ SD043100280
RC393 M16GN@ SD043100280	RC389 M16GN@ SD043100280	RC395 M16GN@ SD043100280	RC391 M16GN@ SD043100280	RC392 M16GN@ SD043100280
RC393 M32G@ SD043100280	RC389 M32G@ SD043100280	RC390 M32G@ SD043100280	RC396 M32G@ SD043100280	RC392 M32G@ SD043100280
RC393 H4G@ SD043100280	RC389 H4G@ SD043100280	RC390 H4G@ SD043100280	RC391 H4G@ SD043100280	RC392 H4G@ SD043100280
RC388 H8G@ SD043100280	RC394 H8G@ SD043100280	RC395 H8G@ SD043100280	RC396 H8G@ SD043100280	RC392 H8G@ SD043100280
RC388 H16G@ SD043100280	RC394 H16G@ SD043100280	RC395 H16G@ SD043100280	RC391 H16G@ SD043100280	RC392 H16G@ SD043100280
RC388 H32G@ SD043100280	RC394 H32G@ SD043100280	RC390 H32G@ SD043100280	RC396 H32G@ SD043100280	RC392 H32G@ SD043100280
RC388 S4G@ SD043100280	RC394 S4G@ SD043100280	RC390 S4G@ SD043100280	RC391 S4G@ SD043100280	RC392 S4G@ SD043100280
RC388 S8G@ SD043100280	RC389 S8G@ SD043100280	RC395 S8G@ SD043100280	RC396 S8G@ SD043100280	RC392 S8G@ SD043100280
RC388 S16G@ SD043100280	RC389 S16G@ SD043100280	RC395 S16G@ SD043100280	RC391 S16G@ SD043100280	RC392 S16G@ SD043100280
RC388 S32G@ SD043100280	RC389 S32G@ SD043100280	RC390 S32G@ SD043100280	RC396 S32G@ SD043100280	RC392 S32G@ SD043100280

CPN R1	SA0000ARD0L	SA0000CMS0L	SA0000ARD0L	SA0000CMS0L	SA0000B70L	TBD	SA0000CYF0L	SA0000BMN0L	SA0000BMN0L	SA0000BZJ0L	TBD	SA0000B6F0L	SA0000B6F0L	SA0000B9K0L	SA0000CHM0L
CPN R3	SA0000ARD2L	SA0000CMS1L	SA0000ARD2L	SA0000CMS1L	SA0000B72L	TBD	SA0000CYF1L	SA0000BMN1L	SA0000BMN1L	SA0000BZJ1L	TBD	SA0000B6F2L	SA0000B6F2L	SA0000B9K1L	SA0000CHM1L
MPN	MT40A512M16LY-075:E	MT40A512M16TB-062:E	MT40A512M16LY-075:E	MT40A512M16TB-062:E	MT40A1G16KNR-075:E	MT40A1G16KD-062:E	MT40A2G16K1L-062:E	HSAN8G6NCR-VKC	HSAN8G6NCR-VKC	HSANAG6NCR-VKC	TBD	K4A8G165WC-BCTD	K4A8G165WB-BCTD	K4AAG165WB-MCTD	K4A8G165WA-MCTD
Memory	4GB	4GB	8GB	8GB	16GB	16GB	32GB	4GB	8GB	16GB	32GB	4GB	8GB	16GB	32GB
Channel	1	1	2	2	2	2	2	1	2	2	2	1	2	2	2
BOM Structure	M4G@	M4GN@	M8G@	M8GN@	M16G@	M16GN@	M32G@	H4G@	H8G@	H16G@	H32G@	S4G@	S8G@	S16G@	S32G@
Die Package	SDP	SDP	DDP	SDP	DDP	DDP	DDP	SDP	SDP	DDP	TBD	SDP	SDP	DDP	DDP
GPIO Pin	Pin Name	Memory Speed	Micron	Micron	Micron	Micron	Micron	Micron	Hynix	Hynix	Hynix	Samsung	Samsung	Samsung	Samsung
GPP_F12	MEM_CONFIG0	2666Mbps	0(RC393)	0(RC393)	0(RC393)	0(RC393)	0(RC393)	0(RC393)	0(RC393)	1(RC388)	1(RC388)	1(RC388)	1(RC388)	1(RC388)	1(RC388)
GPP_F13	MEM_CONFIG1		0(RC394)	0(RC394)	0(RC394)	0(RC394)	1(RC389)	1(RC389)	1(RC389)	0(RC394)	0(RC394)	0(RC394)	1(RC389)	1(RC389)	1(RC389)
GPP_F14	MEM_CONFIG2		0(RC395)	0(RC395)	1(RC390)	1(RC390)	0(RC395)	0(RC395)	1(RC390)	0(RC395)	0(RC395)	1(RC390)	0(RC395)	0(RC395)	1(RC390)
GPP_F15	MEM_CONFIG3		0(RC396)	1(RC391)	0(RC396)	1(RC391)	0(RC396)	1(RC391)	0(RC396)	1(RC391)	0(RC396)	1(RC391)	0(RC396)	1(RC391)	0(RC396)
GPP_F16	MEM_CONFIG4		1(RC392)	1(RC392)	1(RC392)	1(RC392)	1(RC392)	1(RC392)	1(RC392)	1(RC392)	1(RC392)	1(RC392)	1(RC392)	1(RC392)	1(RC392)

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## Bom option


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Version Change List ( P. I. R. List )				Issue	Solution	
Item	Page#	Date	Description	Description	Rev.	
1	9, 14, 52, 58	2019/09/11	Add reserve PCH control bluetooth GPIO solution	1.Add RC510(100K_0201_5%) pull up to +3.3V_ALW_PCH connection to PCH_BT_RADIO_DIS# 2.Change net TOUCH_SCREEN_DET# from UC1.CC35 to UC1.CN23 3.Add net PCH_BT_RADIO_DIS# to UC1.CC35 and RZ301.Pin1 4.Add RZ300, RZ301(0_0201_5%), RZ301 depop 5.Change UE1.A1, RE11.Pin1, RZ300.Pin1 net name from BT_RADIO_DIS# to EC_BT_RADIO_DIS# 6.Add net BT_RADIO_DIS# connect to RZ300.Pin2, RZ301.Pin2, DZ2.Pin1	0.2 (X01)	
2	ALL	2019/09/11	Modified part according to PU and PD power consumption improve plan	1.Change RC401 from 10K_0201_5% to 100K_0201_5% 2.Change RC765 from 10K_0201_5% to 100K_0201_5% 3.Change RC278 from 10K_0201_5% to 100K_0201_5% 4.Change RC567, RC844 from 10K_0201_5% to 100K_0201_5% 5.Change RT80, RT90, RT91, RT92, RT552, RT553, RT554, RT551, RT93, RT94, RT556, RT555 from 10K_0201_5% to 100K_0201_5% 6.Change RR3 from 10K_0201_5% to 100K_0201_5% 7.Change RE704, RE826, RE21 from 10K_0201_5% to 100K_0201_5% 8.Change RC75 from 10K_0201_5% to 100K_0201_5% 9.Change RC220 from 100K_0201_1% to 100K_0201_5%	0.2 (X01)	
3	79	2019/09/11	Modified Part according Dell request	Change RZ1482 from 1M_0201_5% to 330K_0201_5%	0.2 (X01)	
4	43	2019/09/11	Modified TR circuit according confirm with Intel result	Change RT498(10K_0201_5%) from pop to depop	0.2 (X01)	
5	23,24	2019/09/11	Modified DDR circuit to correct	1.Add CD145(10U_0603_10V6M), Pin1 connect to +2.5V_MEM, Pin2 connect to GND 2.Add RD96, RD97, RD98(0_0201_5%) and Pin1 connect to DDR_A_BGL_R, Pin2 connect to GND 3.Add RD99, RD100, RD101(0_0201_5%) and Pin1 connect to DDR_B_BGL_R, Pin2 connect to GND	0.2 (X01)	
6	40	2019/09/11	Modified HDMI circuit to correct	1.Change RV614 from 4.7K_0201_5% to 0_0201_5% 2.Change RV614.Pin1 net name from +3.3V_RUN to TMDS_CFG1 3.Change CV777.Pin1 connection from UV19.Pin46, RV21.Pin1 to RV21.Pin2, UT1.R5, RT184.Pin1	0.2 (X01)	
7	ALL	2019/09/12	Modified part according ESD request	1.Change DV13 from CEST523 to AZ5125 2.Change DV14, DZ10, DZ21 from CEST523 to CEST23 3.Change DT5, DT6, DT9, DT10, DT13, DT14, DT17, DT18, DT55, DT48, DT51, DT49, DT50, DT53, DT54, DT52 from DESD3V3Z to AZ5B8S	0.2 (X01)	
8	ALL	2019/09/12	Modified part according RF request	Remove CV765, CV767, CV766, CV768, CV769, CV770, CV771, CV772, CV773, CV774, CV775, CV776 reserve cap (0.1U_0201_10V6K)	0.2 (X01)	
9	59	2019/09/17	Change Board ID to X01	Change RE79 from 240K_0402_5% to 130K_0402_5%	0.2 (X01)	
10	38	2019/09/17	Change part according ESD request	1.Change DV13 from AZ5125 to L03ESDL5V 2.Change DV14, DZ10, DZ21 from CEST23 to L03ESDL5V	0.2 (X01)	
11	66, 40, 70, 45	2019/09/17	Add part according EMI request	1.Add CZ337(0.1U_0201_25V6K) and Pin1 connect to +3.3V_RUN, Pin2 connect to GND 2.Add CV779(0.1U_0201_25V6K) and Pin1 connect to +3.3V_RUN, Pin2 connect to GND 3.Add CR29(0.1U_0201_25V6K) and Pin1 connect to +3.3V_RUN, Pin2 connect to GND 4.Add CT394, CT395(0.1U_0201_25V6K) and Pin1 connect to +20V_TBTA_VBUS, Pin2 connect to GND	0.2 (X01)	
12	38	2019/09/17	Change touch screen circuit to correct	1.Swap QV23.Pin1 from +3.3V_5V_RUN_QV8 to +3.3V_RUN 2.Swap QV23.Pin3 from +3.3V_RUN to +3.3V_5V_RUN_QV8	0.2 (X01)	
13	8	2019/09/17	Modified G3 sharing WDT circuit to reserved	Change QC9, RC303, CC341 from pop to depop	0.2 (X01)	
14	58	2019/09/17	Change part to reserve	Change RE11(100K_0201_5%) from pop to depop	0.2 (X01)	
15	52	2019/09/17	Modified BT_RADIO_DIS# circuit to correct	1.Delete reserve RZ301(0_0201_5%), Pin1 disconnect PCH_BT_RADIO_DIS#, Pin2 disconnect BT_RADIO_DIS# 2.Add reserve RZ302(100K_0201_5%), Pin1 connect +3.3V_WLAN, Pin2 connect EC_BT_RADIO_DIS# 3.Change DZ2.Pin1 net name from BT_RADIO_DIS# to PCH_BT_RADIO_DIS#, DZ2.Pin2 net name from BT_RADIO_DIS#_R to BT_RADIO_DIS# 4.Delete net name BT_RADIO_DIS#_R 5.Change WL1.Pin63 net name from BT_RADIO_DIS#_R to BT_RADIO_DIS#	0.2 (X01)	
16	58, 74	2019/09/18	Add net for thermal table to define WWAN and Non-WWAN sku according thermal team request	1.Add net WWAN_DET# and connect to UE1.L11, J101.B10 2.Add RE839(100K_0201_5%), Pin1 connect to WWAN_DET#, Pin2 connect to +3.3V_ALW	0.2 (X01)	
17	58, 59	2019/09/19	Add reserve circuit for thermal sensor	1.Add CE80(2200P_0201_25V7K) for reserve, Pin1 connect to UE1.B11 net name is REM_DIODE3_P, Pin2 connect to UE1.A11 2.Add QE30, CE81(100P_0201_50V8J) for reserve 3.REM_DIODE3_P connect to QE30.1, QE30.2 and CE81.1 4.REM_DIODE3_N connect to QE30.3 and CE81.2	0.2 (X01)	
18	9, 38	2019/09/19	Add reserve touch reset circuit	1.Add RZ310(0_0402_5%), Pin1 connect to JTS1.6(TS_RST#_R), Pin2 connect to PCH_PLTRST#_AND 2.Add RZ311(0_0402_5%) for reserve, Pin1 connect to JTS1.6(TS_RST#_R), Pin2 connect to TS_RST# 3.Add net TS_RST#_R connect to JTS1.Pin6, RZ311.1, RZ310.1 4.Add net TS_RST# connect to RZ311.2, UC1.CM24	0.2 (X01)	
19	38	2019/09/19	Add net align with X11 platform	1.Add 3.3V_CAM_EN#_R connect to RZ388.2, CZ220.1, QZ1.2 2.Add 3.3V_TS_EN_R connect to RV326.6, RV323.2, QV7.2, RV324.2 3.Add +5V_RUN_QV7 connect to QV7.1, RV400.1, RV6.2 4.Add +5V_RUN_QV7_R connect to RV400.2, QV8.2, CV635.1	0.2 (X01)	
20	38	2019/09/19	Add reserve LCDVDD enable RC delay circuit	1.Change net name EN_LCDPWR to LCD_PWR_EN and disconnect UV24.Pin4, DV3.Pin1, RV3.1 2.Add RV180(0_0402_5%), CV80(1U_0402_6.3V6K) for reserve 3.LCD_PWR_EN connect to DV3.Pin1, RV180.1 4.Add net LCD_PWR_EN_R connect to RV180.2, CV80.1, RV3.1, UV24.Pin4 5.CV80.2 connect to GND	0.2 (X01)	
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Item	Page#	Date	Description	Description			
1	38	2019/09/27	Change part according follow spyglass MLK	Change RV2 from 4.7K_0201_5% to 2.2K_0201_5%(SD043470180 to SD000012R80)			0.2 (X01)
2	44	2019/10/03	Modified part align with X11 platform	Change RT85(0_0201_5%) from pop to depop			0.2 (X01)
3	74	2019/11/19	Change HDA RF cap from pop to de-pop according fixed audio device lost issue	Change CZ330, CZ332, CZ334, CZ335(47P_0201_50V8J) from pop to depop			0.3 (X02)
4	58	2019/11/19	Modified part according to PD power consumption improve plan	Change RE342, RE56 from 10K_0201_5% to 100K_0201_5%			0.3 (X02)
5	59	2019/12/10	Change Board ID to X02	Change RE79 from 130K_0402_5% to 62K_0402_5%			0.3 (X02)
6	52,58	2019/12/10	Modified BT_RADIO_DIS# circuit	1.Add DZ16(RB751S-40) between on EC_BT_RADIO_DIS# and BT_RADIO_DIS# 2.Change RZ300(0_0201_5%) form pop to depop 3.Change RE11(100K_0201_5%) from depop to pop			0.3 (X02)
7	38,66	2019/12/10	Change part according ESD team request	Change DV13, DV14, DZ10, DZ21, DZ108 from L03ESDLSVOCG3 to CEST523NC5VB			0.3 (X02)
8	64	2019/12/16	Add part according ESD team request	Add CZ380(0.1U_0201_10V6K), Pin1 connect to BATT_WHITE#, Pin2 connect to GND			0.3 (X02)
9	38	2019/12/16	Modify part according EMI team request	Change LV1 from pop to depop, add RV999(0_0402_5%), Pin1 connect N32816135, Pin2 connect BIA_PWM, and colay with LV1			0.3 (X02)
10	52	2019/12/16	Delete reserve location align with X11	Delete RZ302(100K_0201_5%), Pin1 connect +3.3V_WLAN, Pin2 connect EC_BT_RADIO_DIS#			0.3 (X02)
11	66	2019/12/16	Reserve 1.8V setting for future use with new FIPC tool	Add reserve location RZ1600(10K_0201_5%), Pin1 connect +1.8V_PRIM, Pin2 connect TFM_PIRQ#			0.3 (X02)
12	58	2019/12/16	Modify part according EC team request	Change RE838(0_0201_5%) from depop to pop			0.3 (X02)
13	38	2019/12/16	Modify TS circuit for soft start and add discharge circuit	1.Change CV635.Pin1 connection from TS_PWR_EN#_R to +3.3V_5V_RUN_QV8 2.Change CV635.Pin2 connection from GND to TS_PWR_EN#_R 3.Change RV6.Pin2 connection from +5V_RUN to +3.3V_5V_RUN_QV8 4.Change RV6.Pin1 connection from TS_PWR_EN# to TS_PWR_EN#_R 5.Change RV400.Pin1 connection from TS_PWR_EN# to TS_PWR_EN#_R 6.Change RV400.Pin2 connection from TS_PWR_EN#_R to TS_PWR_EN# 7.Add RV775(100_0402_5%) for reserve, Pin1 connect to +TS_PWR, Pin2 connect to +TS_PWR_DIS 8.Add QV100(PJE138K) for reserve, Pin1 connect to +TS_PWR_DIS, Pin2 connect to TS_PWR_EN#_R, Pin3 connect to GND			0.3 (X02)
14	79	2019/12/16	Remove battery switch according Dell request	1.Change QZ2(PJX138K), QZ19(PJE138K), RZ1(100K_0201_5%), RZ2(2M_0201_5%), RZ3(100_0201_5%), RZ4, RZ5(2.2K_0201_5%), LED3, SW4 from pop to depop 2.Change RZ6(0_0201_5%) from depop to pop			0.3 (X02)
15	59	2019/12/17	Add circuit fixed 360 casue auto power on solution	1.Add RE902(10M_0201_1%), Pin1 connect to LID_CL_SIO_TAB#, Pin2 connect to LID_CL#_QE32 2.Add CE401(2.2U_0402_10V6M), Pin1 connect to LID_CL#_QE32, Pin2 connect to GND 3.Add DZ110(RB751S-40), Pin1 connect to N38978302, Pin2 connect to LID_CL#_QE32 4.Add RE903(49.9K_0201_1%), Pin1 connect to LID_CL_SIO_TAB#, Pin2 connect to N38978302 5.Add CE400(1U_0201_6.3V6M) for reserve, Pin1 connect to LID_CL_SIO_TAB#, Pin2 connect to LID_CL_SIO_TAB#_D1 6.Add DZ109(RB751S-40), Pin1 connect to LID_CL_SIO_TAB#, Pin2 connect to LID_CL_SIO_TAB#_D1 7.Add RE904(2M_0201_5%), Pin1 connect to +RTC_CELL, Pin2 connect to LID_CL_SIO_TAB#_D1 8.Add QE32(PJX138K_SOT563-6), Pin1 connect to GND, Pin2 connect to LID_CL#_QE32, Pin3 connect to LID_CL#_D, Pin4 connect to GND, Pin5 connect to LID_CL_SIO_TAB#_D1, Pin6 connect to LID_CL_SIO_TAB#_D1			0.3 (X02)
16	66	2019/12/17	Add Fuse according factory request	Add FZ6(0.5A_65V), Pin1 connect to +3.3V_RUN, Pin2 connect to +3.3V_RUN_FZ6			0.3 (X02)
17	ALL	2019/12/18	Change 0 ohm to short pad(0603)	Change RT508 to short pad			0.3 (X02)
18	ALL	2019/12/18	Change 0 ohm to short pad(0402)	Change RZ1408, RV180, RR20, RC216, RC440 to short pad			0.3 (X02)
19	ALL	2019/12/18	Change 0 ohm to short pad(0201)	Change RC25, RC29, RC582, RC32, RC30, RC27, RC26, RC660, RC337, RC738, RC243, RC532, RC559, RC430, RC157, RC429, RC159, RC153, RC632, RC631, RC425, RZ1423, RC426, RZ1420, RZ120, RD87, RZ388, RV19, RV748, RV634, RV633, RV635, RV750, RV749, RV632, RV751, RT40, RT394, RT105, RT520, RT521, RT78, RT403, RT110, RT548, RT402, RT511, RT79, RT510, RT77, RZ1385, RZ56, RZ827, RE103, RE565, RE104, RE105, RE318, RE608, RE601, RE361, RE290, RE548, RE59, RE602, RE600, RE603, RE102, RE552, RE90, RE275, RCH99, RZ347, RZ346, RCH95, RZ26, RZ400, RZ29, RZ152, RZ153, RZ350, RZ114, RZ112, RZ351, RN129, RN99, RR9, RR10, RR7, RR8, RR6, RA54, RA48, RZ345, RC850, RC736, RZ6, RC851, RZ1415, RC853, RC735, RV628, RC852, RC737, RE30, RC328, RC442, RC215, RT456 to short pad			0.3 (X02)
20	64	2019/12/31	Change LED resistor according ME request	Change RZ361, RZ28 from 1.5K_0402_5% to 1K_0402_1%			0.3 (X02)
21	44	2020/01/06	Change PD circuit MLCC align with NBMLK	Change CT82, CT83 from 1U_0402_25V6K to 2.2U_0402_25V6M(SE000010V00 to SE000013H00)			0.3 (X02)
22	ALL	2020/02/19	Change 0 ohm to short pad(0603)	Change RC422, RC330, RC329 to short pad			1.0 (A00)
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